C 46561

Name.....

Reg. No.....



# EIGHTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
## JUNE 2008

EC 2 K 803—MICROELECTRONICS TECHNOLOGY

Time : Three Hours  Maximum : 100 Marks

I. (a) Explain the principle of water processing, with a neat sketch.

(b) Why Optical exposures are preferred for microelectronic devices ? Explain.

(c) Give an account on "Device and Isolation".

(d) Explain the advantages of schottky contacts.

(e) Enumerate and explain the advantages and applications of CMOs technology.

(f) Enumerate and explain the BICMOS fabrication process.

(g) Explain the layout of MOSFET with a neat sketch.

(h) Explain the design rules for well and pads.

(8 × 5 = 40 marks)

II. (a) (i) Explain the principle of optical lithography in detail with neat sketches. (7 marks)

(ii) Explain the MOCVD process with neat sketches. (8 marks)

*Or*

(b) Explain the following :—

(1) Fick's law. (2) Channelling.

(3) Deal-grove model.

(3 × 5 = 15 marks)

III. (a) Explain in detail the LOCOS and SWAMI processes with neat diagrams.

*Or*

(b) Describe in detail the advantages of schottky contacts and Implanted ohmic contacts with neat sketches.

IV. (a) Describe in detail the CMOS fabrication process sequence with neat sketches.

*Or*

(b) Explain in detail the hot carrier effects in BJT and CMOS with neat sketches.

V. (a) Explain in detail the layouts of NAND and NOR gates with neat sketches.

*Or*

(b) Write short notes on.

(1) Layout of junction Isolated BJT. (7 marks

(2) Layout using Cell hierarchy. (8 marks

(4 × 15 = 60 marks