C 58323

(Pages : 2)

Name......................................

Reg. No...........................

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2009

EC/AI 2K 604—DIGITAL SIGNAL PROCESSING

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

Part A

1. (a) What is causality ? What is the necessary and sufficient condition for causaling of an LIT system ?

   (b) Draw and explain the basic butterfly diagram of DIF radix -2FFT algorithm diagram of DIF radix -2 FFT algorithm.

   (c) What is warping effect ?

   (d) Give the expression for signal to quantization noise ratio and calculate the improvement with an increase of 2 bits to the existing bit.

   (e) Compare the Butterworth and Chebyshev filter.

   (f) What is meant by optimum equiripple design criterion ?

   (g) What do you mean by sub-band coding ?

   (h) What is SIMD and VLIW in DSP processor ?

   (8 × 5 = 40 marks)

Part B

2. (a) (i) Find the response of an L I T system with impulse response $h(x) = \{2, 1, 3\}$ for the input $x(n) = \{1, 2\}$ using DIT radix –2 FFT algorithm.

   (10 marks)

   (ii) State and prove convolution theorem of DFT.

   (5 marks)

   Or

   (b) (i) A discrete time system is characterized by the equation

   $$y(n) = \sum_{k=-2}^{n} 2^{k-n} x(k+1)$$

   Check whether the system is (1) LTI and (2) BIBO stable.

   (8 marks)

   (ii) Show that DTFT of a real value signal is Hermiltain symmetry.

   (7 marks)

Turn over

3. (a) Find the output round off noise power for the system having transfer function

$$H(z) = \frac{1}{(1-0.5z^{-1})(1-0.4z^{-1})}$$

which is realized in cascade form. Assume word length is 4 bits.

Or

(b) Explain signal scaling to prevent overflow limit cycle in the second order digital filter implementation.

(15 marks)

4. (a) (i) Explain the polyphase decomposition for FIR filter structure.   (8 marks)

(ii) What is the principle of designing FIR filter using frequency sampling method.

(7 marks)

Or

(b) (i) Design a band-pass filter which approximates the ideal filter with cut-off frequencies at 0.2 rad/sec and 0.3 rad/sec. The filter order is N = 7. Use Hamming window.

(10 marks)

(ii) Compare the Hamming window and Blackman window.   (5 marks)

5. (a) A multiplier-accumulate, with three pipe stages, is required for a digital signal processor. Sketch a block diagram of a suitable configuration for the MAC. with the aid of a timing diagram. Explain how the MAC works.

Or

(b) Explain how Harvard architecture as used by the TMS 320 family differs from the strict Harvard architecture. Compare this with the architecture of a standard von Neumann processor.

[4 × 15 = 60 marks]