C 58260 (Pages : 2) Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2009

EE 2K 404/PT EE 2K 302 – ELECTRONICS – II

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

I. (a) An amplifier has a gain of 8×10^4 without feedback and a gain of 2×10^4 with feedback. Calculate the amount of negative feedback and the value of feedback factor.

(b) State Barkhausen conditions for sustained oscillations.

(c) A differential amplifier has a typical common mode gain of 35 dB and CMRR of 72 dB. Find the output voltage V_o when the input voltages are 0.16 MV and 0.18 MV.

(d) Draw the output of a differentiator circuit for (i) Sine wave input signal ; (ii) Square wave signal.

(e) List out the applications of a Op-Amp comparator.

(f) Define the terms capture range and lock in range of a PLL.

(g) Mention the drawbacks of a binary weighted resistor D/A converter. How are these limitations removed is a resistor ladder D/A converter.

(h) Design a wide band reject filter having f_H = 400 Hz and f_L = 2 kHz having a pass band gain of 2.

(8 × 5 = 40 marks)

Part B

II. (a) Draw a circuit for a Wein bridge oscillator and explain its operation. Derive the condition for sustained oscillations and also derive an expression for the frequency of oscillations.

Or

(b) Draw the circuit diagram of a voltage shunt feedback amplifier. Draw a small signal equivalent circuit of the same and find out the feedback factor B. Explain briefly how negative feedback is realized in the amplifier.

III. (a) (i) Explain the working of an Op-Amp based instrumentation amplifier. Find out the expression for output voltage of the instrumentation amplifier.

(ii) Design an Op-Amp adder circuit to get the output expression $V_o = -(0.1\,V_1 + V_2 + 10V_3)$ where V_1, V_2 and V_3 are inputs.

(10 + 5 = 15 marks)

Or

(b) Explain the various stages of an Op-Amp block diagram with suitable circuits.

Turn over

IV. (a) Explain the working of a Schmitt trigger circuit and derive an expression for hysteresis.

Or

(b) (i) Design an analog multiplier circuit using log and antilog amplifiers.

(ii) Draw the block diagram of a VCO and explain its operation.

(5 + 10 = 15 marks)

V. (a) (i) List out specifications of a D/A converter.

(ii) Explain working of a Dual slope ADC with a neat block diagram.

(5 + 10 = 15 marks)

Or

(b) Design a fourth order Butterworth Low Pass filter whose bandwidth is 1 kHz.

(15 marks)

[4 × 15 = 60 marks]