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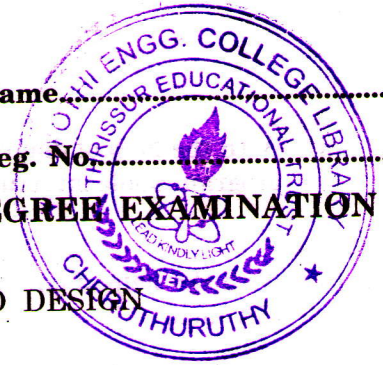
Name.....

Reg. No.....

**FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION  
JULY 2009**

CS/IT 04 : 404—MICROPROCESSOR BASED DESIGN

(2004 Admissions)



Time : Three Hours

Maximum : 100 Marks

*Answer all questions.*

- I. (a) What is meant by wait state ? How it can be introduced ?  
(b) List the various functions provided by the chipset to the mother board.  
(c) Name the default segments and their offset registers of a microprocessor. Also specify the use of each segments.  
(d) What are selectors and descriptors ? What for they are used ?  
(e) Explain how the hidden refresh is done in a DRAM chip.  
(f) Draw the I/O map of the personal computer.  
(g) List the sequence of operations that take place as soon as a valid interrupt is recognized in real mode of operation.  
(h) Explain the function of (i) bus master and (ii) bus arbiter.

(8 × 5 = 40 marks)

- II. (a) What is the need for bus buffering ? Draw the fully buffered 8086/8088 microprocessor diagram and explain.

*Or*

- (b) Describe the features of 8088 in its maximum and minimum mode of operation.

- III. (a) List and explain the different addressing modes supported by 8086 instruction set.

*Or*

- (b) (i) Write an assembly language program using 8086 instructions to convert the binary to ASCII. Also explain the algorithm with an example.

(8 marks)

- (ii) Discuss about the disk organization.

(7 marks)

- IV. (a) Design a memory decoder to fix the address for a 64 K B EPROM interfaced to 8088 from  $F0000_h$  to  $FFFFFF_h$ . Also draw the interface circuit diagram. Use 2764 EPROM which is organized  $8 K \times 8$ .

*Or*

- (b) Name and explain the different modes of operation of 82055 Programmable Peripheral Interface (PPI) chip.

Turn over

V. (a) With the help of diagram explain how the interrupt structure can be expanded using 8259A programmable interrupt controller.

Or

(b) With the help of circuit diagram, explain how a pair of ADC chip can be interfaced through ISA bus.

[4 × 15 = 60 marks]