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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third semester B.Tech degree examinations (S) September 2020

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN (EC, AE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) i. Convert the hexadecimal number 2FC3 into binary and decimal. (5)

ii. Write down the Octal equivalent of hexadecimal number 3A2E.

iii. Subtract binary number 10110 from 10001001

b) Write down the 1's and 2's complement of the following numbers. (6)

i. – 4

ii. +253

iii. – 181

c) Determine the Hamming code for the information 1011, with even parity. (4)

2 a) Using the Boolean theorems simplify the following expressions. (8)

(i) $Y = \bar{A}C\overline{(\bar{A}BD)} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$

(ii) $Y = A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C$

b) Using K map simplify the SOP function, and realize it using only NAND gates. (7)

f(a,b,c) = Σm (0,2,3,4,5,6)

3 a) Realize a 2 bit comparator. (7)

b) Implement the following function using an 8 X 1 MUX. (8)

F(A,B,C,D) = Σm (1,3,4,11,12,13,14,15)

PART B

Answer any two full questions, each carries 15 marks.

4 a) List any four performance ratings of TTL family. (4)

b) Draw the circuit of a CMOS inverter and explain its working (4)

c) Explain the working of a master slave JK flipflop, with the help of circuit diagram. (7)

5 a) Explain the working of a 3 bit UP/DOWN counter. (7)

b) Implement the following two Boolean functions with a PLA: (8)

F1(A,B,C) = Σm (0,1,2,4)

F2(A,B,C) = Σm (0,5,6,7)

6 a) Describe the working of a 3 bit TTL NAND gate in totem pole configuration. (8)

b) Convert a D flipflop into a JK flipflop, showing all the steps. (7)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain the working of a 4 bit PISO register. Draw the circuit and timing diagram. (10)

b) Draw the Moore sequential model. How it differs from Mealy machine. (5)

c) For the Mealy Model State table is given below draw the state diagram. (5)

PS		NS				O/P	
		X=0		X=1		X=0	X=1
Y1	Y2	Y1	Y2	Y1	Y2	Z	Z
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

8 a) Explain the working of a 4 bit twisted ring counter, with the help of timing diagrams. (10)

b) For the state tables of the machines given below, find the equivalence partition and a corresponding reduced machine. (10)

PS	NS,Z	
	X=0	X=1
A	B,1	H,1
B	F,1	D,1
C	D,0	E,1
D	C,1	F,1
E	D,1	C,1
F	C,1	C,1
G	C,1	D,1
H	C,0	A,1

9 a) Draw the state diagram, state transition table and state equation using D flip flop for the given state table. (10)

PS	NS		O/P	
	X=0	X=1	X=0	X=1
A(00)	A	B	0	0
B(01)	C	B	0	0
C(10)	A	D	0	0
D(11)	C	B	1	0

b) Design a synchronous counter using T flipflop to count the following sequence. (10)
0-3-1-4-6-0

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