C 58190 (Pages 3) Name.................................

Reg. No.................................

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2009

EC 04 404—COMPUTER ORGANIZATION AND ARCHITECTURE

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

I. (a) Give the RTL description of the restoring and nonrestoring division schemes with suitable illustrations.

(b) Give a formal proof of correctness of padding bits for the arithmetic shift operation on negative numbers expressed in 1's and 2's complement notation.

(c) Microprogrammed control is not suitable for RISC architecture. Justify the validity or otherwise of this statement.

(d) Evolve a suitable hardware structure to implement dynamic microprogramming using a write able control store.

(e) Organize the subfields of MAR to realize a block set associatively mapped cache main storage hierarchical memory with MS capacity of 16 K pages of 16 word each and cache capacity of 256 pages divided into sets, each set having 8 pages.

(f) A set associative mapping cache has a set size of 4. The cache capacity is 2K words and that of main storage is 128 K × 32. Derive all pertinent information required to design the cache memory and note the data path for the set associative organization. Determine the average memory access time for a cache hit ratio of 0.85, cache access time of 100 n sec and main storage access time of 500 n sec.

(g) Make a comparative study of the three different modes of IO transfer programmed, DMA and interrupt IO.

(h) Describe the typical schemes employed for bus interfacing while transferring

(i) Serial data.

(ii) Parallel data.

(8 × 5 = 40 marks)

II. (a) Design an array of cells intended to implement 2's complement combinational array multiplier using Booth's algorithm. Give the cell details and the array structure showing input and output signals. Assume 4 bit multiplier and multiplicand.

(15 marks)

Or

Turn over

(b) Design the logic circuit for the correction step of the non-restoring division method. Note the behaviour with proper explanation of steps and terminologies used.

(15 marks)

III. (a) Design the data path to implement normalize instruction on 32 bit floating point data with 8 bit exponent, 24 bit sign magnitude mantissa and hexadecimal base. Clearly state the assumptions, if there are any, for the design.

(15 marks)

Or

(b) Design a microprogrammed and also hardwired control unit for bit pair multiplication scheme. Give the data path and control path with binary listing of the microprogram. Use resource encoding for the control field in microprogrammed controller.

(15 marks)

IV. (a) A virtual memory system has 16 K word logical address space, 8 K word physical address space with a page size of 2 K words. The page address trace of a program has been found to be :

7 5 3 2 1 0 4 1 6 7 4 2 0 1 3 5

Note the four pages resident in the memory after each page reference change for each of the following replacement policies :

(i) FIFO.

(ii) LRU.

(iii) Anticipatory swapping.

(15 marks)

Or

(b) Design an intelligent page transfer scheme between a cache memory and main storage having following specifications :

(i) 4 word cache page, each word of 4 bytes.

(ii) bus width of 32 bits and bus transfer time of 50 n sec.

(iii) 4 module main storage with cycle time of 200 n sec.

Give the timing diagram for write back transfer scheme.

(15 marks)

V. (a) Define each of the following IO control methods, programmed IO, DMA controllers, IOPs. List the advantages and disadvantages of each method with respect to program design complexity, IO bandwidth and interface hardware costs.

(15 marks)

Or

(b) Instructions such as store instructions that modify memory make it difficult to support precise interrupts in pipelined CPUs. Why is this so ? Outline a design method to solve this problem.

(15 marks)

[4 × 15 = 60 marks]