C 58189

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Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2009

EC 04 403—DIGITAL ELECTRONICS

(2004 Admissions)

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

Part A

I. (a) Convert the logic function into mid-terms $y = A + \overline{B} + C + \overline{D}$.

(b) Draw the block diagram of fast adder and explain.

(c) Explain what is meant by noise immunity of digital IC ?

(d) Explain the operation of Johnson counter with neat circuit diagram.

(e) Describe the design procedure for asynchronous sequential circuits.

(f) Differentiate static-0 and static-1 hazards.

(g) Compare Moore and Mealy models.

(h) Explain about one-hot statement assignment.

($8 \times 5 = 40$ marks)

Part B

II. (a) Obtain the simplified expression in sum-of-products and product-of-sum form :

$$F(A, B, C, D, E) = \sum(0, 1, 4, 5, 16, 17, 21, 25, 29).$$

Or

(b) Design a combinational circuit that converts a decimal digit from the BCD code to excess - 3 code.

III. (a) Draw the circuit of an ECL logic for OR gate and explain its operation.

Or

(b) Draw the circuit of 4 bit synchronous counter using JK flip-flop and explain its operation with truth table.

Turn over

IV. (a) Derive a minimal state table for a single-input and single-output Moore type FSM that produces an output of logic '1', if in the input sequence it detects either 110 or 101 pattern overlapping sequence should be detected.

Or

(b) For the following table assume that the unspecified outputs in states B and G use 0 and 1, respectively. Derive the minimized state table for this FSM.

Present State		Next State		Output Z	
		$w = 0$	$w = 1$	$w = 0$	$w = 1$
A	....	B	C	0	0
B	...	D	–	0	–
C	...	F	E	0	1
D	...	B	G	0	0
E	...	F	C	0	1
F	...	E	D	0	1
G	...	F	—	0	–

V. (a) Obtain a hazard-free minimum cost implementation of the function.

$$F(x_1, x_2, x_3, x_4) = \sum m(0, 4, 11, 13, 15) + \sum d(2, 3, 5, 10).$$

Or

(b) Design an asynchronous sequential circuit with two inputs X and Y one output Z. The output should be 1 if the number of 1 inputs on X and Y together since reset is a multiple 4 and 0 otherwise. Realize the circuit with state assignments : 00, 01, 11, 10 and using D flip-flops.

(4 × 15 = 60 marks)