C 56283 (Pages : 2) Name.....

Reg. No.....

EIGHTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2009

CS 04 802 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

1. What are Instruction Set Architecture and list out its types?
2. Write about Pipeline Hazards.
3. How Paralleism is implemented in Instruction Level?
4. Differentiate Parallel Processing and Vector Processing.
5. List out the features and advantages of using Virtual Memory.
6. What is Program Locality?
7. Write about Multiprocessors.
8. What is Memory Consistency?

(8 × 5 = 40 marks)

Part B

1. (a) Discuss about performance measurement. (7 marks)

   (b) Explain in detail about how to Encode an Instruction set. (8 marks)

Or

2. Write about the practical difficulties while we Implementing Data and Control Hazards. (15 marks)

3. Explain the following :–

   (a) Dynamic Scheduling. (7 marks)

   (b) Multiple Issues of Instructions. (8 marks)

Or

4. Discuss in detail about vector Architecture and its characteristics. (15 marks)

5. Write short notes on following :–

   (a) Cache Misses and Miss penalty. (8 marks)

   (b) Performance Measures. (7 marks)

Or

Turn over

6. Explain in detail about I/O system design and its Reliability, Availability.

(15 marks)

7. Explain in detail about Loosly Coupled and Tightly Coupled Architecture.

Or

8. Explain in detail about Synchronisation.

(15 marks)

[4 × 15 = 60 marks)