Reg No.:_____ 00000EC361121902 Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fifth semester B.Tech degree examinations (S) September 2020

Course Code: EC361

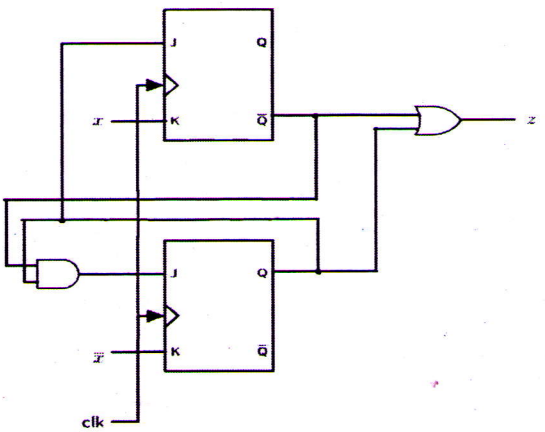
Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Examine the clocked synchronous sequential network given below and obtain the excitation equation, excitation table, state transition table, state table and state diagram. (10)



b) Draw the ASM chart for mod-8 down counters. (5)

2 a) Obtain a primitive flow table and minimal-row flow table for a fundamental mode asynchronous sequential network with two inputs x1, x2 and one output z. The inputs x1 and x2 never change simultaneously. The output is same as x2 if x1 = 1. However if x1 = 0, the output should remain fixed at its last value. (10)

b) With a transition table, explain the concept of critical race, non-critical race and cycle. (5)

3 a) Explain the three steps in state table reduction. (6)

b) Find the reduced flow table for the following: (9)

PS	NS Input State (x1x2)				Output (z) Input State (x1x2)			
	00	01	10	11	00	01	10	11
A	Ⓐ	B	E	-	1	-	-	-
B	A	Ⓑ	-	H	-	0	-	-
C	G	-	Ⓒ	-	-	-	1	-
D	Ⓓ	F	C	-	0	-	-	-
E	A	-	Ⓔ	-	-	-	1	-
F	D	Ⓕ	-	H	-	0	-	-
G	Ⓖ	B	C	-	1	-	-	-
H	–	F	C	Ⓗ	-	-	-	1

PART B

Answer any two full questions, each carries 15 marks.

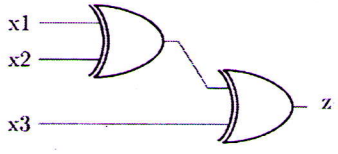
4 a) What is an essential hazard? Explain its impact with the help of a logic diagram. (5)

b) Examine the problem of switch bouncing and explain the remedial solution. (5)

c) Explain the functionality of mixed operating mode circuit. (5)

5 a) Using Kohavi algorithm, find the test set to detect SA0 and SA1 faults in a circuit whose function is f(a,b,c,d) = ad' + c'd + a'c (9)

b) Find the test vectors for the SA0 and SA1 faults on each of the input lines by path sensitization method for the 3 bit parity checking logic circuit shown below: (6)



6 a) Describe Kohavi Algorithm for multiple fault detection (10)

b) Explain clock skew? Differentiate between positive clock skew and negative clock skew. (5)

PART C

Answer any two full questions, each carries 20 marks.

7 a) In the context of PLA, explain the terms: i) growth faults ii) shrinkage faults iii) appearance faults iv) disappearance faults. (8)

b) Use IISc algorithm to determine the essential prime cubes of the four-variable single-output function, f = 2201 + 0102 + 0111 + 0110 + 2100 (12)

8	a)	With a diagram, describe the I/O block of XC4000 FPGA	(8)
	b)	Explain the following terms: i) PLA minimisation ii) PLA folding iii) Foldable Compatibility Matrix	(9)
	c)	Illustrate the XC4000 general interconnect structure.	(3)
9	a)	List the differences between FPGA and CPLD	(2)
	b)	With illustrations, describe the architecture of XC9500 CPLD family.	(8)
	c)	With suitable sketches, describe the internal structure of XC4000 CLB.	(10)

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