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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fifth semester B.Tech degree examinations (S) September 2020

Course Code:EE365

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

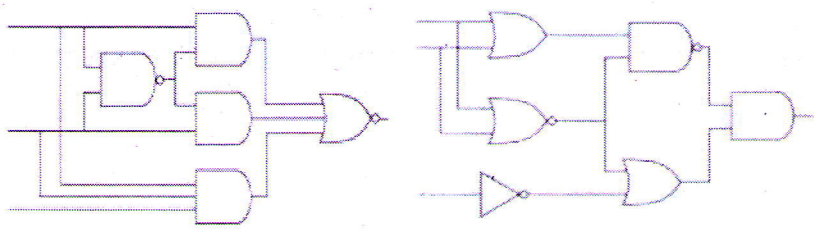
Answer all questions, each carries5 marks. Marks

1		Define Design Automation and explain the tasks to be performed by EDA tools?	(5)
2		Explain the basic structure of VHDL Code?	(5)
3		With the help of suitable block diagram explain the different models of synchronous sequential systems?	(5)
4		Write VHDL code for negative edge T-FF? ***(Assume Necessary data if Required)***	(5)
5		Explain VHDL simulation cycle?	(5)
6		With the help of suitable example, explain the concept of inferred Latch in synthesis of process statements	(5)
7		With the suitable diagram describe four types of cross point fault that can occur in a PLA consisting of AND and OR Plane	(5)
8		With the help of suitable diagram explain the architecture of Built in logic block observation (BILBO)	(5)

PART B

Answer any two full questions, each carries 10 marks.

9	a)	Explain the basic architecture of FPGA?	(5)
	b)	Compare signal and variable in VHDL?	(5)
10		Explain the role of Test bench in VHDL? Write VHDL test bench to test all combination of 8:1 Multiplexer?	(10)
11		Derive Boolean expressions for the circuits of Figure shown below; use truth tables to discover if they are equivalent. Assume inputs A, B, & C.	(10)



PART C

Answer any two full questions, each carries 10 marks.

12 Derive state diagram and hence draw the ASM chart for mod-6 counter (10)
(Assume Necessary data if Required)

13 With the help of necessary timing diagram explain the operation of dynamic RAM and hence write its VHDL Code? (10)

14 a) Explain the salient features of ASM chart (5)

b) Identify the circuit that can generate the following sequence and hence write VHDL code for obtaining the same ***(Assume Necessary Data, if required)*** (5)
"1000","1100","1110","1111","0111","0011","0001","0000",.....

PART D

Answer any two full questions, each carries 10 marks.

15 The following sequence of operations is part of a cube root solution routine: (10)

```
a <= x * x;
a <= 3 * a;
b <= y / a;
a <= 2 * x;
a <= a / 3;
c <= a – b;
```

Convert this sequence to single assignment form and hence construct a data dependency graph. Assuming that each arithmetic operation takes exactly one clock cycle, derive an unconstrained as late as possible (ALAP) schedule.

16 What are different styles of design that should be avoided and different modifications methods to enhance the testability of that design? (10)

17 a) With the help of suitable example explain resources constraints during synthesis? (5)

b) Explain the phases involved in path sensitization based automatic test pattern generation (ATPG) scheme. (5)

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