

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth semester B.Tech examinations (S), September 2020

**Course Code: EC206****Course Name: COMPUTER ORGANISATION (EC)**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer any two full questions, each carries 15 marks*

Marks

- 1 a) Draw the block diagram of a 16-bit ripple carry adder using full adders. Calculate the delay of a 32-bit ripple carry adder. Assume a full adder delay is 200ps. (7)
- b) Express the following base 10 numbers in 16-bit fixed-point two's complement format with eight integer bits and eight fraction bits. Express in IEEE 754 single-precision floating-point format also. Express your answer in hexadecimal. (8)
- (a) -20.5 (b) 24.25
- 2 a) Explain any two assembly instruction formats in MIPS with examples. (6)
- b) Write the operation performed in MIPS processor when it executes the following instructions (9)
- (a) add \$t0, \$s4, \$s5
(b) lw \$t2, 32(\$0)
(c) sw \$s1, 4(\$t1)
- 3 a) Draw the symbol and implementation of a 4 x 4 multiplier. (7)
- b) Discuss about operands and registers of MIPS processor. Write the use of \$0, \$gp, \$sp and \$t8. (8)

PART B*Answer any two full questions, each carries 15 marks*

- 4 a) Explain five addressing modes of MIPS with example. (15)
- 5 a) Draw the datapath for single cycle processor for *sw* instruction. (9)
- b) List the characteristics of single-cycle and multi cycle microarchitectures. (6)
- 6 a) How does a multicycle processor address the weakness of single-cycle processor? (7)
- b) Explain the steps involved in executing a high level language program. Draw the flow chart. (8)

PART C

Answer any two full questions, each carries 20 marks

- 7 a) Explain any two modes of data transfer between the processor/memory and I/O devices in a computer system. (6)
- b) Draw the internal organization of a DRAM cell and explain the read and write operation. (8)
- c) Illustrate virtual address to physical address translation using page table. (8)
- 8 a) Define miss rate and average memory access time. (6)
- b) Draw the internal organization of a SRAM cell and explain the read and write operation. (8)
- c) Compute the size of a 4096-word x 32-bit memory array. Also find the width of address and data bus. (6)
- 9 a) Describe temporal locality and spatial locality with respect to cache memory. (6)
- b) Illustrate how data is found in a $C=8$ word, 2-way set associative cache (10)
- c) Draw the internal organization of a 4×3 memory array. (4)
