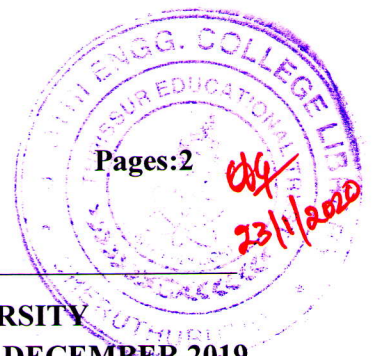


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**APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019**

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

- 1 Give the relevance of MAR, PC and IR in a typical computer system with neat diagram. 3
- 2 Differentiate between Big-endian and Little-endian assignment for word addressing. 3
- 3 Illustrate the advantages of using multiple bus organization over single bus organization with the help of a sample instruction execution. 3
- 4 Divide 25 by 8 using restoring division algorithm. 3

PART B

Answer any two questions, each carries 9 marks

- 5 a) Define Addressing mode and explain Different types of addressing modes with an example for each. 6
- b) Show the effect of stack operations on the stack with diagram. 3
- 6 a) What is meant by instruction sequencing? Discuss the different types of instruction sequencing with example. 4
- b) Illustrate Booth multiplication with an example 5
- 7 a) Discuss the data path inside the processor with single bus organization with neat diagram 4
- b) Write down the control sequence for the execution of the instruction *Add (R1), R2* in single bus organization 5

PART C

Answer all question, each carries 3 marks

- 8 Discuss the different ways of accessing I/O devices of a computer system. 3
- 9 Explain the daisy chain method with neat diagram 3
- 10 Justify the need of memory hierarchy in a computer and discuss the various parameters that are considered for the formation of memory hierarchy. 3
- 11 Discuss about different types of RAMs. 3

PART D*Answer any two questions, each carries 9 marks*

- 12 a) What is interrupt? Discuss the differences between subroutine and interrupt service routine. 4
- b) Describe the different bus arbitration techniques for DMA data transfer. 5
- 13 a) Explain semiconductor ROM memories 4
- b) Discuss the SCSI protocol for a complete disk read operation by listing out the sequence of events involved in it. 5
- 14 a) How do you relate set associative mapped cache with Direct mapped and associative mapped cache mechanisms? 3
- b) Design a 64K x 8 memory module using 16K x 1 static memory chips. 6

PART E*Answer any four questions, each carries 10 marks*

- 15 a) Write short notes on Arithmetic , logic and shift microoperations with examples 6
- b) Show the block diagram that executes the following conditional control statements
- $C \cdot T_2 : F \leftarrow A$ 4
- $C T_2 : F \leftarrow B$ where C is the conditional variable and A, B, F are registers
- 16 Draw the block diagram of a processor unit with 16 selection variables and discuss the functions of selection variables. Derive the control word for the micro operation $R1 \leftarrow R1 - R2$. 10
- 17 Discuss the major operations that can be performed by a parallel adder in the design of arithmetic circuit. 10
- 18 Discuss the different methods of control logic design in detail 10
- 19 Describe the organization of micro program sequencer with neat diagram. Also provide its address sequencing capabilities. 10
- 20 Explain the horizontal and vertical microinstructions in microprogrammed control. 10
