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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries3 marks. Marks

1 Represent decimal number $(5.75)_{10}$ in single precision floating point format. (3)

2 Simplify the Boolean function **F= AB'+AB+BC**. Draw the circuit using basic gates. How many logic gates do you save by simplification? (3)

3 Show the three different representations for a negative decimal number N = -25 in binary. (3)

4 Obtain the two canonical forms of the Boolean function F(A,B,C)=**A'B+BC'+BC+AB'C'** (3)

PART B

Answer any two full questions, each carries9 marks.

5 a) Simplify the given Boolean function using Karnaugh Map and obtain the minimum Sum Of Products expression. F(WXYZ)=Σ(3,5,6,7)+d(10,11,12,13,14,15) (5)

b) Verify or contradict the statement "NAND logic function is commutative but not associative" using truth table. (4)

6 a) Convert the following numbers to binary and perform subtraction both 2's complement and 1's complement. (5)
1)Minuend $(3A)_{16}$, subtrahend $(24)_{16}$
2)Minuend $(24)_{16}$, subtrahend $(3A)_{16}$

b) Obtain the simplified Product of Sums expression for the function F(ABC)=π(0,2,3,5,7) using Karnaugh Map. (4)

7 a) A keyboard contains 26 uppercase letters and 10 decimal digits as keys. The keys are arranged as a two-dimensional matrix. Each key should be identified by a unique binary code. Propose a suitable coding scheme for the keyboard layout. And write the code for letter H. (5)

b) A digital circuit has four inputs and one output. The output is equal to 1 when (1) all the inputs are equal to 1 or (2) none of the inputs are equal to 1 or (3) an odd number of inputs are equal to 1
a) obtain the truth table b) Find the simplified output function in sum of products. (4)

PART C

Answer all questions, each carries3 marks.

8 What is the function of a half subtractor circuit? Write the logic expression for the outputs. Draw the logic diagram of half subtractor. (3)

9 What is the advantage of edge triggering over level triggering in flipflops? (3)

10 Draw the diagram of a JK latch using NOR gates. Explain the working of the latch when both J and K inputs are active simultaneously. (3)

11 Draw the schematic diagram of a 3-bit parallel adder. What is the drawback of this circuit? (3)

PART D

Answer any two full questions, each carries9 marks.

12	a)	What is a multiplexer? Draw the internal diagram of a 4X1 multiplexer, clearly indicating the inputs and outputs. Explain the functionality using the function table	(4)
	b)	Draw the circuit of a master slave JK flipflop. With the help of a timing diagram explain its working.	(5)
13	a)	Implement the function F(A,B,C)=Σ(0,1,4,6) using a 4X1 multiplexer.	(5)
	b)	What is meant by excitation table of a flip flop? Obtain the excitation table of RS flipflop.	(4)
14	a)	Design a BCD to Excess-3 code convertor using a 4-bit parallel adder.	(5)
	b)	Draw the block diagram of a sequential circuit and differentiate synchronous and asynchronous sequential circuits.	(4)

PART E

Answer any four full questions, each carries10 marks.

15	With the help of timing diagram and logic diagram, explain the working of Serial In Serial Out shift register and Parallel In Serial Out shift register using an example.	(10)
16	Draw the logic circuit of a BCD ripple Counter and explain its working with a timing diagram	(10)
17	Show the internal architecture of a 8X4 ROM. Show the implementation of a full adder using ROM.	(10)
18	What is meant by a PLA? Show the implementation of F1=AB'C+AC+BC and F2= AC +BC+B'C using a suitable PLA.	(10)
19	Design a synchronous counter using T flipflops having states 000-001-011-101-110-111-000.	(10)
20	What is meant by Hardware Description Languages? Give examples. Write the HDL code for a 4X1 multiplexer	(10)

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