Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SIXTH SEMESTER B.TECH DEGREE EXAMINATION(S), DECEMBER 2019

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) With a neat sketch, explain the process of ion implantation for IC fabrication. (8)

b) Draw schematic and explain any two CVD processes. (7)

2 a) With the help of neat diagram explain crystal growth in Czochralski process. (7)

b) Define photolithography and discuss various steps involved in photolithographic process. (8)

3 a) A Si sample is covered with 0.25μm thick SiO_2 layer. Find the time required to grow an additional 0.2μm thick SiO_2 at 1200□ by dry oxidation. For dry oxidation at 1200□ B = 0.045 μm, B/A = 1.120 μm/hr, τ = 0.027 (5)

b) Solve Fick's law for pre deposition diffusion. (3)

c) List various methods of resistor fabrication. (7)

PART B

Answer any two full questions, each carries 15 marks

4 a) The VTC of an inverter is given in Figure 1. (4)

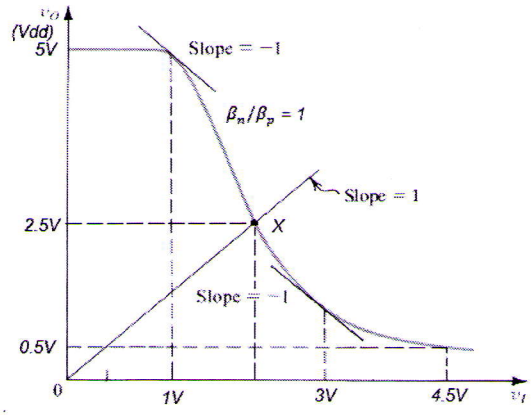

Figure 1.

Define the terms Noise Margin Low and Noise Margin High. Calculate their numerical values.

b) Calculate drain current for the region marked X in Figure 1. Given $V_{tn} = |V_{tp}| =$ $0.5V$ and $\beta_n = 1mA/V^2$. (3)

c) Draw the circuit of NMOS pass transistor logic. Discuss its output characteristics and comment on the drawbacks. (8)

5 a) For a two input CMOS NOR gate, draw (10)

i. Circuit diagram

ii. Stick diagram

iii. Layout

b) Implement the logic function **(AB + C(A+D))'** using CMOS logic. (5)

6 a) Draw the switching characteristics of CMOS inverter and discuss the terms associated with it. (6)

b) Realize an XOR gate using (9)
   i. CMOS logic
   ii. NMOS pass transistor logic
   iii. Transmission gate logic

PART C

Answer any two full questions, each carries 20 marks

7 a) Draw the circuit diagram of a 6T CMOS SRAM cell. Briefly explain the read and write operations by drawing simplified models. (10)

b) Implement a full adder using complementary static CMOS. Explain the merits and demerits associated with the circuit. (10)

8 a) Draw and explain the internal architecture of an FPGA. List four applications of FPGA. (10)

b) With block diagrams, illustrate the behaviour of linear carry select adder and square root carry select adder. (10)

9 a) How does a sensing amplifier contribute to the operation of an SRAM? With a circuit diagram, explain how differential sensing is applied to an SRAM memory column. (10)

b) Show the conversion of a ripple carry adder into a carry bypass adder. Draw the block diagram of a 16 bit carry bypass adder and show the worst-case delay path. (10)

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