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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: EC361

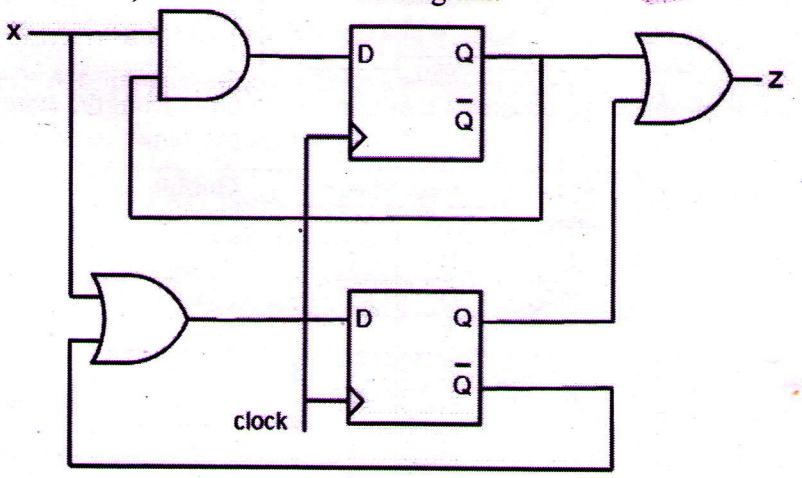
Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Study the CSSN shown below and obtain the excitation expressions, excitation/ state transition table, state table and state diagram. (9)



b) Generate an ASM chart for a Mealy network that detects non-overlapping sequence of 101. (6)

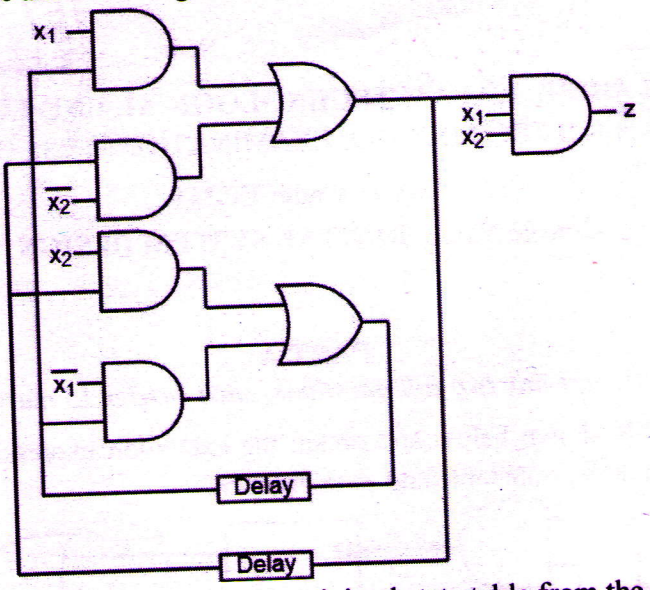
2 a) Find the reduced flow table from the primitive flow table of a fundamental mode asynchronous sequential circuit given below. (9)

Present State	Next state				Output			
	x=00	x=01	x=10	x=11	x=00	x=01	x=10	x=11
a	c	a	b	-	-	0	-	-
b	-	a	b	e	-	-	1	-
c	c	a	-	d	0	-	-	-
d	c	-	b	d	-	-	-	0
e	f	-	b	e	-	-	-	1
f	f	-	-	e	1	-	-	-

b) Explain critical and non-critical races in asynchronous sequential circuits with the aid of an appropriate state transition table. (6)

3 a) Examine the ASC shown below to generate the excitation/transition table, state (7.5)

table, flow table and flow diagram.



b) Using implication charts, construct a minimal state table from the state table given below. (7.5)

Present State	Next State		Output
	X=0	X=1	
A	B	C	1
B	D	E	0
C	A	F	0
D	E	C	0
E	G	H	1
F	B	H	1
G	D	F	0
H	F	E	1

PART B

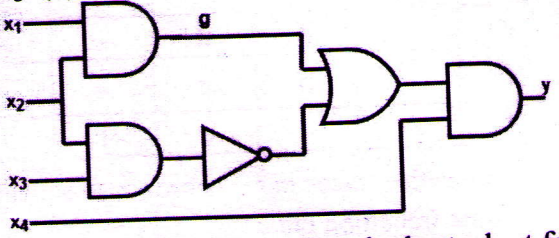
Answer any two full questions, each carries 15 marks.

4 a) Draw the logic circuit diagram of the SOP expression $f=\sum(2,3,6,7,11,12,13,15)$. Examine the possibility of hazards in the circuit. Explain how the hazard can be detected and eliminated with the aid of Karnaugh map. (7.5)

b) Explain essential hazards in asynchronous sequential circuits. (7.5)

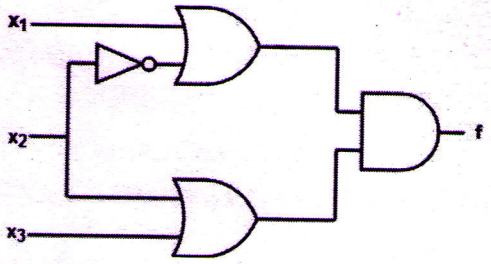
5 a) For the circuit given in figure below, find the test vectors for the following faults using path sensitization. (7.5)

(i) SA0 at x_3 (ii) SA1 at x_3 (iii)SA0 at g (iv) SA1 at g.



b) Construct a table listing the set of all possible single stuck-at faults and the faulty (7.5)

and fault-free responses of the circuit shown below. Also find the fault cover table and identify the minimal complete test set.



6 a) Describe the operation of data synchronizers with the help of suitable timing diagrams. (7.5)

b) Find the test vectors for all SA0 and SA1 faults in the circuit whose Boolean function is $f=x_1x_2+x_2'x_3+x_3x_4'$ using Kohavi algorithm. (7.5)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Explain PLA folding. Define foldable compatibility matrix and state its properties. (12)

b) Determine the minimal test set for PLA $f = x_1x_2+x_2x_4+x_1x_3'x_4'$ (8)

8 a) Describe the simplified block diagram of configurable logic block of XC4000 FPGA family. (10)

b) Explain the switch matrix of Xilinx 9500 CPLD family with the help of a diagram. (10)

9 a) Explain various test generation techniques of PLA. (10)

b) With a suitable diagram, describe the input-output block architecture of Xilinx 9500 CPLD family. (10)

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