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Pages:2

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(R&S), DECEMBER 2019

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks.

Marks

1 What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers? (3)

2 Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. (3)

(i) 10011 - 10010 (ii) 100010 - 100110

3 Find the complement of the following expressions: (3)

(i) xy' + x'y (ii) (a + c) (a + b') (a' + b + c')

4 State and Prove Absorption law in Boolean Algebra. (3)

PART B

Answer any two full questions, each carries 9 marks.

5 (a) The value of a float type variable is represented using a single precision 32 bit floating point format IEEE 754 standard that uses 1 bit for the sign , 8 bits for biased exponent and 23 bits for the mantissa. A float type variable X is assigned value of -0.0625 .What is the representation of X in hexadecimal notation? (6)

(b) Perform the following operations (3)

(i) Find the 16's complement of C3DF.

(ii) Convert C3DF to binary.

(iii) Find the 2's complement of the result in (ii)

6 (a) Add and multiply the following numbers without converting them to decimal. (6)

(i) Binary numbers 1011 and 101.

(ii) Octal numbers 62 and 37

(iii) Hexadecimal numbers 2E and 34.

(b) Represent the unsigned decimal numbers 791 and 658 in BCD, and then show the steps necessary to form their sum. (3)

7 (a) We can perform logical operations on strings of bits by considering each pair of corresponding bits separately (called bitwise operation). Given two eight- bit strings A = 10110001 and B = 10101100, evaluate the eight- bit result after the following logical operations: (3)

(i) AND (ii) OR (iii) XOR

(b) Simplify the following Boolean expressions to a minimum number of literals: (6)

(i) x'yz + xz (ii) (x + y) (x + y') (iii) xyz + x'y + xyz'

PART C

Answer all questions, each carries3 marks.

8 Design a combinational circuit with three inputs and one output. The output of the circuit is 1 when the decimal value of the inputs is less than 3. The output is 0 otherwise. (3)

9 Implement the Boolean function **F(A, B, C, D) = π(3, 7, 12)** with a multiplexer: (3)

10 Differentiate between Combinational and Sequential circuits. Give two examples for each. (3)

11 Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter. (3)

PART D

Answer any two full questions, each carries9 marks.

12 (a) Design a four-bit 2's complementer combinational circuit. The circuit accepts a 4-bit binary number as input and generates the 2's complement of the input. Show that the circuit can be constructed with exclusive-OR gates. (7)

(b) Predict what the output functions are for a five-bit 2's complementer? (2)

13 (a) Show that the characteristic equation for the complement output of a JK flip-flop is: $Q'(t+1) = J'Q' + KQ$ (3)

(b) Draw the logic diagram of a 4x16 decoder constructed with two 3x8 decoders (4)

(c) Implement T flip- flop using NAND gates. (2)

14 A sequential circuit has two JK flip-flops A and B and one input x . The circuit is described by the following flip-flop input equations: (9)

$J_A = x$ $K_A = B'$ $J_B = x$ $K_B = A$

(i) Tabulate the state table.

(ii) Draw the state diagram of the circuit.

(iii) Derive the state equations for A(t+1) and B(t+1)

PART E

Answer any four full questions, each carries10 marks.

15 (a) Draw and explain the different types of shift registers. (6)

(b) Explain how shift registers can be used for serial transfer. (4)

16 Design and construct a Johnson counter with 8 distinguishable states. Give its timing diagram. (10)

17 (a) Design a synchronous counter with the following repeated binary sequence 000, 100,111, 010, 011 using T Flip Flops. (6)

(b) Write a note on error detection and correction. (4)

18 Find the minimum size of PLA required to implement the following functions? $F(X,Y,Z) = \Sigma m\ (1,3,5,7)$, $G(X,Y,Z) = \Sigma m\ (0,2,4,6)$ (10)

19 (a) Design a BCD ripple counter using T flipflops (6)

(b) Explain the implementation of full adder using Hardware Description Language (HDL). (4)

20 Draw and explain the flow chart for addition and subtraction of two binary numbers in sign magnitude form. (10)