

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SIXTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: EC304

Course Name: VLSI

Max. Marks: 100

Duration: 3 Hours

PART A*Answer any two full questions, each carries 15 marks*

Marks

- 1 a) How electronic grade silicon is prepared from raw SiO_2 ? (5)
- b) Illustrate the dry and wet oxidation technique used in IC fabrication with schematic diagram. (10)
- 2 a) With the help of mathematical equations, explain the distribution of impurities in a semiconductor in ion implantation process. (10)
- b) Phosphorous is implanted in a p-type silicon sample with a uniform doping concentration of 5×10^{16} atoms per cm^3 . If the beam current density is $2.5 \mu\text{A}$ per cm^2 and the implantation time is 8 minutes, calculate the implantation dose and peak impurity concentration. Assume $\Delta R_p = 0.3 \mu\text{m}$ (5)
- 3 a) Explain N-well CMOS IC fabrication sequence with the help of neat diagrams. (10)
- b) Explain one method of fabrication of capacitor structure in integrated circuits. (5)

PART B*Answer any two full questions, each carries 15 marks*

- 4 a) Explain the various types of power dissipation in CMOS inverter? Derive the expression for total power consumption of a CMOS inverter. (10)
- b) Why PMOS transistor can pass only strong ones and NMOS can pass strong zeros. (5)
- 5 a) Draw the circuit diagram and layout of a two input CMOS NAND gate. (10)
- b) Implement the function $u = A'B + AB'$ and $v = AB + A'B'$ using complementary pass transistor logic. (5)
- 6 a) Explain the structure and working of a transmission gate. Implement 4×1 multiplexer using transmission gates. (10)
- b) Implement the function $f = [AB + C(DE + F)]'$ using static CMOS logic. (5)

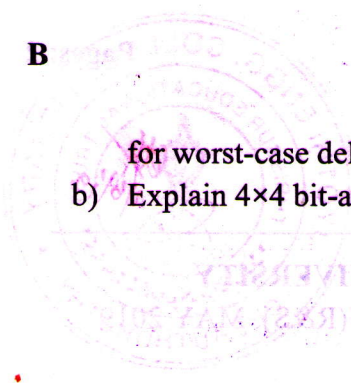
PART C*Answer any two full questions, each carries 20 marks*

- 7 a) Explain the read and write operation of a six transistor CMOS SRAM cell. (10)
- b) What is FPGA? Explain its constructional details with diagram. What are the advantages of FPGA? (10)
- 8 a) Design a 4-bit \times 4-bit NOR-based ROM array and explain its working. (10)
- b) Explain the read and write operation of a three-transistor DRAM cell. (10)
- 9 a) Explain the working a 16-bit carry-by pass adder and write down the expression (10)

for worst-case delay.

b) Explain 4x4 bit-array multiplier with block diagram.

(10)



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PART A

Answer any two full questions, each carries 15 marks

- 1. The electronic grade silicon is prepared from low SiO₂. (2)
- 2. Illustrate the dry and wet oxidation technique used in IC fabrication with schematic diagram. (10)
- 3. With the help of mathematical equations explain the distribution of impurities in a semiconductor in ion implantation process. (10)
- 4. Phosphorus is implanted in a p-type silicon sample with a uniform doping concentration of 3×10^{17} atoms per cm³. If the beam current density is 2.5 μ A per cm² and the implantation time is 5 minutes, calculate the implantation dose and post-implantation concentration. Assume $\sigma = 1.5 \times 10^{-16}$ cm². (2)
- 5. Explain the well CMOS IC fabrication sequence with the help of neat diagrams. (10)
- 6. Explain the method of fabrication of capacitor structure in integrated circuits. (2)

PART B

Answer any two full questions, each carries 15 marks

- 1. Explain the various types of power dissipation in CMOS inverter. Derive the expression for total power consumption of a CMOS inverter. (10)
- 2. What is a CMOS pass transistor and how can pass transistors be used to pass strong zeros? (2)
- 3. Derive the circuit diagram and layout of a two input CMOS NAND gate. (10)
- 4. Implement the function $y = A'B + AB'$ and $y = AB + A'B'$ using complementary pass transistors. (2)
- 5. Explain the structure and working of a transmission gate. (10)
- 6. Implement a 4-bit multiplier using transmission gates. (2)
- 7. Implement the function $F = (A + B)(C + D)$ using static CMOS logic. (2)

PART C

Answer any two full questions, each carries 10 marks

- 1. Explain the read and write operation of a six transistor CMOS SRAM cell. (10)
- 2. What is FTQA? Explain its constructional details with diagram. What are its advantages? (10)
- 3. Design a 4-bit x 4-bit NOR-based ROM array and explain its working. (10)
- 4. Explain the read and write operation of a three-transistor DRAM cell. (10)
- 5. Explain the working of a 16-bit carry-propagate adder and write down the expression. (10)