Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION(R&S), MAY 2019

Course Code: EC212

Course Name: LINEAR INTEGRATED CIRCUITS AND DIGITAL ELECTRONICS (MC)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks. Marks

1 List and explain the characteristics of Op-Amp. (5)

2 Differentiate between PAL and PLA. (5)

3 Comment on clippers and clampers using Op-Amp IC. (5)

4 Using Boolean algebra, verify $AB + \overline{A}C+BC = AB+\overline{A}C$ (5)

5 Obtain an expression for first order low pass filter (LPF). (5)

6 Draw the logic diagram of a master- slave J-K flip-flop using NAND gates and Explain how the race around condition is eliminated in it. (5)

7 Distinguish between half adder and full adder. Give the truth table and logic circuit of half adder and full adder. (5)

8 Design a 4 bit ring counter using JK flip flop and also draw its output waveform. (5)

PART B

Answer any three full questions, each carries 10 marks.

9 Elucidate in detail the working of a monostable and astable multivibrator using Op-Amp IC 741. (10)

10 a) Explain how an Op-Amp works as a differentiator. (5)

b) Interpret the following (5)

i)V-I converter with floating load

ii) V-I converter with ground load

11 a) How a 4 bit R-2R ladder DAC works? (5)

b) Define A/D converter and explain any one of its type. (5)

12 Draw the circuit of a Log and Antilog amplifier using Op-Amp and derive its output voltage. (10)

13 Minimize the following using K-map

a) $F(A,B,C,D) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ (10)

b) $F(P,Q,R,S) = \pi (3, 5, 7, 8, 10, 11, 12, 13)$

PART C

Answer any two full questions, each carries 15 marks.

14 a) Implement the following Boolean function F(A, B, C, D)= Σ m (0, 1, 2, 3, 4, 10, 11, 14, 15) by using 8X1 multiplexer. (9)

b) What is a multiplexer? Draw a logic diagram and logic symbol of a 4 to 1 MUX with the help of truth table. (6)

15 Design and implement a 4 bit synchronous up counter by using JK flip flops. (15)

16 a) Design and implement a 4 bit binary to gray code converter. (10)

b) Design and implement a 3-to-8 decoder. (5)

17 a) Design a sequence detector that produces an output '1' whenever the non overlapping sequence 1011 is detected (10)

b) Draw a 4 bit binary asynchronous up counter. (5)

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