Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIFTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code:EE365

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks. Marks

1		Define EDA and its functions.	(5)
2		What are identifiers? Explain different types of identifiers with example.	(5)
3		Define three components in an ASM chart and its representation.	(5)
4		Write the simplest VHDL model for a positive edge triggered D flip-flop.	(5)
5		Explain non-synthesisable VHDL constructs with example.	(5)
6		What is Behavioural synthesis?	(5)
7		Define two approaches for testing a digital circuits.	(5)
8		What is the basic principle behind fault modelling? Explain fault models	(5)

PART B

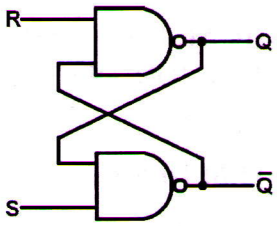
Answer any two full questions, each carries 10 marks.

9	a)	Describe overall design flow of RTL synthesis based design with the help of block diagram	(5)
	b)	Write the VHDL model for n to 2^n decoder with shift operators	(5)
10	a)	With the help of connection diagram explain CMOS inverter and CMOS NAND gate.	(5)
	b)	Derive the VHDL model for 4 to 1 multiplexer.	(5)
11	a)	Explain the basic structural difference between FPGA and CPLD with the help of neat block diagrams.	(5)
	b)	Write the VHDL model for 2 to 4 decoder.	(5)

PART C

Answer any two full questions, each carries 10 marks.

12	a)	Given below the diagram and truth table of a SR latch. Model this in VHDL	(5)



Truth table of SR latch.

S	R	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	$\overline{Q}$

b) Explain the difference between Mealy machine and a Moore machine. (5)

13 a) A state machine has two inputs, A and B, and one output, Z. If the sequence of input pairs of the order A=1 B=1, A=1 B=0, A=0 B=0 is detected, Z becomes 1 duringthe final cycle of the sequence, otherwise the output remains at 0. Draw state diagram and write a twoprocessVHDL model of a state machine to implement this system. (10)

14 a) With example describe how a ROM device is modelled in VHDL? (5)

b) Explain how positive edge-triggered behaviour can be described in VHDL. (5)

PART D

Answer any two full questions, each carries 10 marks.

15 a) What assumptions are made by the single-stuck fault model (5)

b) Explain some of the simulation modelling issues which should be taken care while doing simulation. (5)

16 a) Explain event driven simulation. (5)

b) Explain the principles involved in SISO testing method and identify the benefits and costs involved. (5)

17 a) Explain with examples what is meant by a constraint in RTL synthesis. (5)

b) Explain built-in self-test (5)

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