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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FOURTH SEMESTER B.TECH DEGREE EXAMINATION, DECEMBER 2018

Course Code: CS202

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each carries 3 marks.

1		Write the three-address, two-address and one-address representations of the operation below with relevant assumptions: **C ← [A] + [B]**	3
2		What is the use of linkage register in subroutine invocation?	3
3		Why is non-restoring division faster than restoring division?	3
4		Design and draw a 3X2 array multiplier.	3

PART B

Answer any two questions. Each carries 9 marks.

5		Illustrate various addressing modes with proper examples. Which is the default addressing mode selected by assemblers and compilers and why?	9
6		Give the flow chart for Booth's Algorithm. Illustrate using an example.	9
7	(a)	Assuming that stack grows towards lower address range write assembly code for the following (Without using PUSH and POP) : (i) Pushing elements stored at ITEM1, ITEM2 onto stack (ii) Popping an element onto address ITEM (iii) Copying value of top of stack to address TOP	4.5
7	(b)	Compare and contrast single bus and multiple bus organisation of CPU.	4.5

PART C

Answer all questions. Each carries 3 marks.

8		Compare the two main modes of DMA transfer.	3
9		Explain any two interrupt priority schemes.	3
10		What is MFC signal? How is it related to Memory Access Time?	3
11		Which design feature of SRAM cells helps in value retention without refresh?	3

PART D

Answer any two questions. Each carries 9 marks.

12 Illustrate with an example SCSI bus arbitration and selection. 9

13 With the help of a diagram examine the internal organisation of bit cells in a memory chip. 9

14 (a) Explain the architecture of USB with help of a diagram. 4.5

14 (b) Differentiate Direct and Associative mapped cache with examples. 4.5

PART E

Answer any four questions. Each carries 10 marks.

15 Give a simple design for generating status bits for a 8-bit ALU. 10

16 Draw a labelled block diagram of a processor unit with seven registers R1 to R7,a status register,ALU with 3-selection variables and C_{in}, and shifter with 3 selection variables. 10

17 With the help of a flowchart for sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control unit. 10

18 Using a block diagram analyse the design of a microprogram control for a processor unit.

19 What is a control word? With the help of proper illustrations and assumptions show how a designer would compose a control word for the processor unit. 10

20 With the help of a diagram establish the functioning of microprogram sequencer in a microprogram controlled processor. 10

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