Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

			Marks
1		Perform the following operations: i) $(E39)_{16} + (3F9)_{16}$ ii) $(721)_8 - (32)_8$ iii) BCD addition of 0110 0111 and 0101 0011	(3)
2		Perform the following conversions: (Show the steps of conversion) i) $(463.25)_{10}$ to binary ii) $(36.25)_{10}$ to octal iii) $(AF9.0C)_{16}$ to binary	(3)
3		Using Boolean postulates simplify the following expressions: i) x+x'y ii) xy+x'z+yz iii) x'y'z+x'yz+xy'	(3)
4		Express the following functions: i) F_1=AB+B'C in sum of Minterms form. ii) F_2=A+B'C in product of Maxterms form.	(3)

PART B

Answer any two full questions, each carries 9 marks

5		Perform subtraction of the following using r's complement and (r-1)'s complement methods: i) $(7235)_{10}$- $(346)_{10}$ ii) $(1000100)_2$- $(1110100)_2$	(9)
6		Given F(A, B,C,D)= ∑(1, 4, 6, 7, 8, 9, 10, 11, 15). Simplify using Quin-McClusky method and determine the prime implicants, essential prime implicants and the minimized Boolean expression.	(9)
7	a)	Using K-map, simplify the Boolean function F in sum of products form, using the don't care conditions d: F(w, x, y, z) = w' (x'y + x'y' + xyz) + x'z'(y+w) d(w, x, y, z)= w'x (y'z + yz') + wyz	(5)
	b)	Give the IEEE Single precision format for floating point number representation with explanation. Determine the floating-point binary number represented by the following single precision floating point representation. "1100 1010 1100 0111 0001 0000 0011 1011"	(4)

PART C

Answer all questions, each carries 3 marks

8		Implement F= A(B+CD) +B'C with NAND gates.	(3)
9		Derive the simplified Boolean output functions of a full subtractor.	(3)
10		Explain the terms: i) Race-around condition ii) Edge triggering of flip-flops	(3)

11 Implement D flip- flop using NAND gates and explain its working. (3)

PART D

Answer any two full questions, each carries 9 marks

12 a) Implement a 4- bit magnitude comparator. Give a Boolean function to check the equality relation of a pair of bits and derive logic functions for the outputs of the magnitude comparator. (5)

b) Give the characteristic table and excitation table of RS flip-flop and JK flip flop. (4)

13 a) Implement the function with a multiplexer: $F(A, B,C,D) = \sum (0, 1, 3, 4, 8, 9, 15)$ (5)

b) Explain state table and state diagram with an example. (4)

14 a) What is a Master-slave flip-flop? Explain its working with a timing diagram. (4)

b) How can the principle of look- ahead carry reduce the carry propagation time in a binary parallel adder? Derive the Boolean functions for the carry outputs at different stages of a look-ahead carry generator. (6)

PART E

Answer any four full questions, each carries 10 marks

15 Design a BCD ripple counter. Also verify its operation by means of a timing diagram. (10)

16 a) Explain PLA with a block diagram. (4)

b) Design a counter that has a repeated sequence of the following six states: 000, 001, 010, 100, 101, 110 (6)

17 a) Explain the various types of ROMs (4)

b) Implement a 4- bit bidirectional shift register with parallel load. (6)

18 a) Sketch the block diagram of a BCD adder. Using a truth table derive the condition for correction in BCD addition. (5)

b) Design a serial adder using a full adder and shift registers. (5)

19 a) Explain the construction of a 32 X 4 ROM with a logic diagram. (5)

b) Give the logical configuration of shift registers. With a block diagram, explain the use of shift registers for serial transfer of data. (5)

20 Draw a flow chart and explain the addition/ subtraction of two binary numbers in signed magnitude representation. (10)

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