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EIGHTH SEMESTER B.TECH. (ENGINEERING) [2014 SCHEME] DEGREE EXAMINATION, APRIL 2018

Computer Science Engineering

CS/IT 14 801—COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Time: Three Hours

Maximum: 100 Marks

Part A

Answer any eight questions. Each question carries 5 marks.

- (1) Enumerate the tasks of a computer designer.
- (2) What is the use of compiler?
- (3) What is the need for dynamic scheduling?
- (4) Bring out the purpose of an interpreter.
- (5) Write short notes on enhancing vector performance.
- (6) What do you mean by cache miss?
- (7) Write short notes various protection mechanisms for virtual memory.
- (8) Write a short note on protection in Intel Pentium Processor.
- (9) What do you mean by Internet?
- (10) Distinguish between a uniprocessor and a multiprocessor.

 $(8 \times 5 = 40 \text{ marks})$

Part B

Answer all questions.

(11) (a) Explain in detail about quantitative principles of compiler design.

Or

- (b) With a neat sketch, explain in detail about DLX Architecture and its pipelining mechanisms.
- (12) (a) Explain in detail about Instruction Level Paralleism concepts and challenges encountered in the same.

Or

(b) With a neat sketch explain in detail about vector processing and its architecture.

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(13) (a) Explain in detail the memory hierarchy design with a neat sketch.

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- (b) Explain in detail about a case study on Unix File System performance.
- (14) (a) Explain in detail about the practical issues in connecting more than two computers.

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(b) Explain in detail about various application domains of multiprocessor.

 $(4 \times 15 = 60 \text{ marks})$

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- riogram bridging tal in richten Manneton ausmey seinn rios eile W. W.
 - (8) Write a shore option protection in total Pentium Percence.
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 - 101) Distinguish between a unipersonated and a couldnot coessor.

(REMARK) (ALE THE 8)

Part

Analyst all questions.

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(12) (a) English is detail about instruction Level Parallelam concepts and challenges encountered in the same.

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(b) With a seas exercit explain in signal about vector processing and its acciutecture.

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