APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

Q.P. Code: CSP0817141-J (Pages: 2) Name.....

Reg. No.....

FIRST SEMESTER M.TECH. DEGREE EXAMINATION DEC 2017

08EC6241/08EC6541 DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Branch: Electronics & Communication Engineering

(Common to CESP & ECE)

Time:3 hours **Max.marks: 60**

Answer all six questions. Part 'a' of each question is compulsory.

Answer either part 'b' or part 'c' of each question

Q.no.	Module 1	Marks
1.a	Write a note on Fetch and Execute packets	3
	Answer b or c	
b	With neat block diagram explain TMS320C6713 architecture	6
c	Discuss pipelining for TMS320C6713 with an example	6

Q.no.	Module 2	Marks
2.a	Describe register indirect addressing mode	3
	Answer b or c	
b	Write a c program to calculate $1^2+2^2+3^2+....N^2$ with assembly function	6
c	Write c program with c callable assembly function to find sum of products two array	6

Q.no.	Module 3	Marks
3.a	Conceptualize DSP system design environment	3
	Answer b or c	
b	What do you meant by a cross compiler? . Explain different stages to produce	6

executable file from high-level or assembly code

c	Illustrate with block diagram of AIC23 Stereo codec	6

Q.no.	Module 4	Marks
4.a	summarize the hamming and blackman window functions	3
	Answer b or c	
b	Discuss about various Filter design techniques	6
c	Design a FIR Low pass filter with matlab	6

Q.no.	Module 5	Marks
5.a	List the features of adaptive filters	4
	Answer b or c	
b	Explain how a real time digital filter implement using DSP	8
c	Determine DFT(8 point) for a continuous time signal $x(t)=\sin(2\pi ft)$ where f=50Hz	8

Q.no.	Module 6	Marks
6.a	Enumerate the significance of DSP controllers to implement real time systems	4
	Answer b or c	
b	Explain how a simple voice detection and play back system designed using DSP processor	8
c	With neat block diagram explain the implementation of PLL with a DSP processor	8