APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

Q. P. Code : 3BC171 **(Pages: 3)** **Name :.....**

Reg. No: *.....

THIRD SEMESTER M.TECH. DEGREE EXAMINATION December 2017

Branch: Computer Science **Specialization: Computer Science and Engineering**

08CS7021(C) ADVANCED ARCHITECTURE

Time:3 hours **Max.marks: 60**

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Q.no.	Module 1	Marks
1.a	Explain hardwired control unit and its operation in the case of ADD instruction.	3
	Answer b or c	
b	Develop the micro code for LOAD instruction (TWO bus architecture).	6
c	Design a concrete RTN and control signals for the LOAD instruction in a single bus , two bus three bus SRC micro architecture and compare their performance assuming 10% overhead in the latter two architectures .Also draw diagrams for these three architectures.	6

Q.no.	Module 2	Marks
2.a	(i) Explain the advantages of multi level cache organisation? (ii) Compare split cache and unified cache	3
	Answer b or c	
b	Explain write invalidate and write update caches .Give examples to explain the operation of these caches..	6
c	What is cache coherence ? What are the typical states of a cache line in implementing cache coherence ?Explain any one model.	6

Q.no.	Module 3	Marks
3a	Give examples for the following and justify your answer. a. Data dependence b. Name dependence c. Control dependence	3

Answer b or c

b The following instructions are executed using Tomasulos Algorithm. Explain the implementation of Tomasulos Algorithm and show the instruction status, reservation station and register result status at clock no 10. Assume, 3 Add R S units, 3 Load R S units and 2 Mult R S units are available. Load/Sore takes 2 cycles, ADD takes 2 clock cycles, MULT takes 6 clock cycles and DIV takes 10 clock cycles for execution — **6**

```
L.D    F6, 34(R2)
L.D    F2, 45(R3)
DIV.D  F6, F6, F2
ADD.D  F10, F4, F6.
MUL.D  F8, F4, F2
SUB.D  F4, F6, F2
```

c The following program segment is executed using Thomasulos algorithm with Reorder buffer(ROB),with two adders,two load/store unit and two Mul/Div units . With the help of suitable diagrams discuss the advantages of using ROB . Show how ROB is updated.. — **6**

```
LD F0, 10(R2)
ADDD F10,F4,F0
MULD F2,F10,F6
BNE F0, 0, L
ADDD F0,F4,F6
ST F4, 0(R3)
```

Q.no.	Module 4	Marks
4.a	What are homogeneous and heterogeneous cores?	3

Answer b or c

b	Discuss the design choices available for multi core chips.	6
c	Explain a typical multi core architecture with advanced pipelining and memory system components.	6

Q.no.	Module 5	Marks
5.a	Explain various possibilities of multithreading in a multi core processor.	4

Answer b or c

b	(i)	Explain Simultaneous multi threading	8
	(ii)	Discuss the trade off between coarse grained and fine grained computations	
c	(i)	What is load balancing?	8
	(ii)	What are the limitations of multi threading ?	

Q.no.	Module 6	Marks
6.a	With the help of suitable examples, explain the following features of OpenMP. a) sections b) atomic c) barrier d) reduction	4
	Answer b or c	
b	(i) Explain with suitable examples how critical section can be implemented in OpenMP. (ii) Explain with suitable examples how multiple tasks can be executed concurrently in OpenMP	8
c	Write an OpenMP program to perform multiplication of two matrices. Include the properties of work sharing construct Explain how it works.	8