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C 30153 (Pages : 2) Name.....

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SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE (2014 SCHEME) EXAMINATION, NOVEMBER 2017

Electronics and Communication Engineering

EC 14 703—DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **eight** *questions.*

1. (i) What are the delays supported by VHDL ?

   (ii) What is an concurrent signal assignment statement in VHDL ? Give an example.

   (2 + 3 = 5 marks)

2. What is subprogram overloading ? Explain.
3. Briefly mention the differences between Mealy state machine and Moore state machine with simple example.
4. What is clock skew ? Explain.
5. State and explain the rules for state assignment.
6. Summarize the differences between Programmable Read Only Memory (PROM), Programmable Array Logic (PAL) and Programmable Logic Array (PLA) with simple structural examples.
7. Explain the Generic structure of an FPGA.
8. With neat sketch explain the dedicated carry logic of XC 4000 series FPGAs.
9. Explain Bridging Fault with an example.
10. Explain controllability and observability.

(8 × 5 = 40 marks)

Part B

11. (a) (i) Design a Full Adder and write its VHDL code using structural modeling.

    (ii) Explain the usage of process statement with a suitable example.

    (10 + 5 = 15 marks)

Or

(b) (i) Explain configurations and packages in VHDL.

(ii) Write the VHDL code to realize a priority encoder using data flow modelling.

(8 + 7 = 15 marks)

Turn over

12. (a) (i) Explain any one state reduction method.

(ii) Explain Metastability.

(10 + 5 = 15 marks)

Or

(b) (i) Explain static 0 and static 1 hazard. (5 marks)

(ii) Design a sequence detector to defect the sequence 101.

(10 marks)

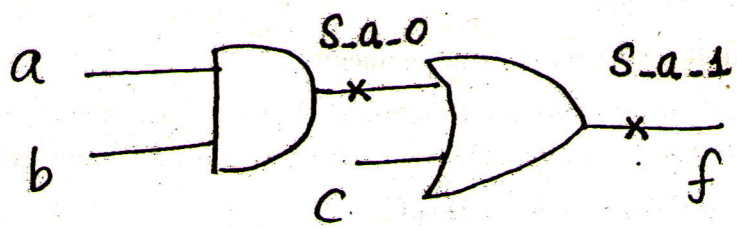
13. (a) Design 2-bit updown counter and implement it using PAL 16 R4. (Required Portion of PAL 16 R4 can alone be illustrated).

Or

(b) Explain the CLB of XC 4000 FPGA with neat sketch.

14. (a) (i) Explain Fault equivalence and Fault dominance with suitable examples.

(ii) Derive the test to detect the following single stuck-at faults :



(5 + 10 = 15 marks)

Or

(b) (i) Discuss in detail about Built-In self-test techniques.

(ii) With neat sketch, explain boundary scan architecture.

(8 + 7 = 15 marks)

[4 × 15 = 60 marks]