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Reg. No._____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JULY 2017

EC203: SOLID STATE DEVICES (AE, EC)

Max. Marks:100. Duration: 3 Hours

PART A

Answer any One from Qn. No.2 and 3. Qn. No. 1 is Compulsory.

1. a) Plot the Fermi Dirac distribution function versus Energy for different temperatures. Justify the plot using necessary equations. (5)

   b) Show that L_n is the average distance an electron diffuses before it recombines. (5)

   c) Derive the expression for conductivity of a Semiconductor. (5)

2. a) For the given data, calculate hole and intrinsic carrier concentrations. Also sketch the band diagram. $N_C = 10^{19} cm^{-3}$, $N_V = 5x10^{18} cm^{-3}$, $E_g = 2eV$, $T = 900^0 K$, $n = 10^{17} cm^{-3}$ (5)

   b) Define Hall Effect. Derive the expressions for i) majority carrier concentration ii) mobility. (5)

   c) Prove that the minimum conductivity of a semiconductor occurs when $n_o = n_i(\mu_p / \mu_n)^{0.5}$. Also find the expression for minimum conductivity. (5)

OR

3. a) A p-type Si with minority electron lifetime of 0.1μs, is uniformly illuminated by a light having photon energy of 2.5eV.

   i) Determine the rate of excess carrier generation that is required to generate a uniform electron concentration of 10^{10} cm^{-3}. (2)

   ii) What is the optical power (cm^{-3}) that should be absorbed to create the excess carrier population of part (i)? (2)

   iii) How much optical power per cm^3 will be generated if the carriers recombine via photoemission? (2)

   b) Derive Steady state diffusion equations. (6)

   c) State and explain the different recombination mechanisms. (3)

PART B

Answer any One from Qn. No.5 and 6. Qn. No. 4 is Compulsory.

4. a) Draw the energy band diagrams of a pn junction when it is i) under equilibrium ii) forward biased iii) reverse biased. (6)

   b) Draw the energy band diagram of a metal-n type semiconductor with $\varphi_m > \varphi_s$ when it is i) under equilibrium and ii) when it is biased. Is the contact rectifying or ohmic? Justify your answer. (6)

   c) What is the difference between depletion and diffusion capacitance in a diode? Which one dominates in forward bias? (3)

5. a) Derive the expressions for i) Contact potential ii) transition region width iii) maximum value of electric field. (8)

   b) A p^+n Si diode has $N_A=10^{15}cm^{-3}$ and $N_D=10^{17}cm^{-3}$, area of cross section $A=10^{-3}cm^2$ and the lifetime in n and p regions be 1 μs at 300K. Determine the diode current for applied voltage of i) V = 0.1V ii) V = 0.6V. Given $D_p = 10cm^2/s$, $D_n = 36cm^2/s$. (4)

   c) What are the assumptions taken for the derivation of the general form of Diode equation? (3)

OR

6. a) A Schottky barrier diode is formed by depositing tungsten on n-type Si. If $N_D = 10^{15}cm^{-3}$, $q\varphi_m = 4.9eV$, $q\chi_s = 4.15eV$ (electron affinity of silicon), at 300K, determine:

   i) Built in Voltage ii) width of depletion region and iii) Maximum electric field. (6)

   b) Draw and explain the characteristics of a tunnel diode. (4)

   c) Derive the expression for the time variation of voltage across a p-n junction as it is switched from forward bias to reverse bias condition. (5)

PART C

Answer any One from Qn. No.8 and 9. Qn. No. 7 is Compulsory.

7. a) Illustrate the minority carrier distribution in a PNP transistor in the active mode of operation. Give values of minority carrier concentrations in the three region. (4)

   b) Define Early effect. What is its effects on I_c, I_B, α and β of a transistor? (4)

   c) Draw the band diagrams for ideal MOS structure at i) equilibrium ii) accumulation iii) depletion and iv) Inversion. (8)

   d) Draw the structure of a FINFET . Plot its output characteristics. (4)

8. a) Derive the terminal current equations of a npn transistor. List the assumptions made for the derivation. (12)

   b) Define with expressions i) Base transport factor ii) Emitter injection efficiency iii) Current transfer ratio iv) Base to collector current amplification factor. (8)

OR

9. a) Draw and explain the capacitance- voltage characteristics of an n-channel MOS capacitor. (5)

   b) What are the effects of real surfaces on the threshold voltage of a MOS capacitor? Derive the threshold voltage equation of a real MOS capacitor? (10)

   c) An n^+-polysilicon gate n-channel MOS transistor is made on a p-type Si substrate with $N_a = 10^{15}cm^{-3}$. The SiO_2 thickness is 100Å in the gate region, at the onset of inversion. Find i) width of depletion layer and ii) V_T. Given ε_r of Si and SiO_2 are 11.8 and 3.9 respectively. (5)

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