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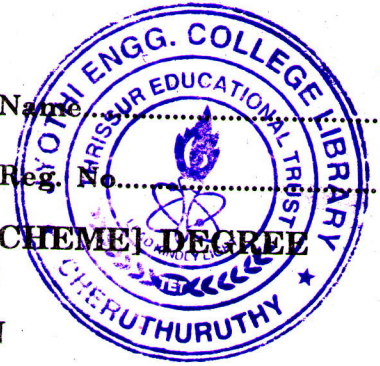
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Name

Reg. No.

**FIFTH SEMESTER B.TECH. (ENGINEERING) [14 SCHEME] DEGREE
EXAMINATION, NOVEMBER 2016**

EE 14 505—DIGITAL SYSTEM DESIGN



Time : Three Hours

Maximum : 100 Marks

Part A

Answer eight questions out of ten questions.

1. List the operators allowed in VHDL languages.
2. Explain data flow style and behavioral style of modeling VHDL with an suitable example.
3. Develop VHDL code for 4×1 multiplexer using three state logic.
4. Briefly explain the rules to perform bubble to bubble logic.
5. Write a VHDL code to model D Flip Flop.
6. What are pipelined output ?
7. What are FPGA ? List the merits and demerits.
8. Write a short note on feedback sequential circuit analysis.
9. Give VHDL code for 4 input NAND gate.
10. Explain the package declaration in VHDL.

(8 × 5 = 40 marks)

Part B

11. Explain in detail about types, constants and arrays in VHDL. (15 marks)

Or

12. (a) Illustrate the steps involved in VHDL design flow. (7 marks)

- (b) Using wait statement, write code to generate waveform in test bench program. (8 marks)

13. Write a VHDL code to make a Generic comparator that compares two n-bit numbers A and B gives the three outputs as G, E, L for $A > B$, $A = B$ and $A < B$ respective. (15 marks)

Or

14. Discuss the salient features of circuit timing diagram and propagation delay. (15 marks)

Turn over

15. Design a synchronous sequential circuit that functions as detector a sequence of 110011 using JK Flip Flop.

(15 marks)

Or

16. Write the VHDL code of state machine to detect the sequence "1001" on a data input then produce a logic '1' output when the sequence has been detected. Overlaps must be considered.

(15 marks)

17. - Discuss the features of 9500CPLD family.

(15 marks)

Or

18. Explain in details about algorithmic state machine.

(15 marks)

[4 × 15 = 60 marks]