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SEVENTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, NOVEMBER 2016

EC/PTEC 09 704—DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Define timing margin in sequential logic diagram.
2. What is meant by adders in VHDL ?
3. Define PLD.
4. What does a 'X' represent on a PLD diagram ?
5. What is meant by clock period ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Explain the Huffman model of a sequential circuit ?
7. Design a VHDL program for a 9 input parity checker.
8. Describe the three state outputs in VHDL.
9. Explain modes of operation of GAL 22V10.
10. Differentiate FPGA and Gate arrays.
11. Describe about Transition table.

(4 × 5 = 20 marks)

Part C

Answer section (a) **or** *section (b) of each question.*

12. (a) A sequence detector with one Input, x and one output, w, is to be designed. The circuit searches on its x input for a sequence of 1011. If in four consecutive clocks the sequence is detected, then its output becomes 1 for exactly one clock period. The circuit continuously performs this search andit allows overlapping sequences. Design state diagram for above application.

Or

(b) Describe the state reduction techniques in a sequential circuit.

Turn over

13. (a) Describe Hamming error correction using behavioural VHDL program.

Or

(b) Explain the VHDL program with four 8-bit three state drives.

14. (a) Explain the PROM architecture which makes it possible for PLD.

Or

(b) Describe the characteristics of Bipolar sequential PLD.

15. (a) Describe the Basic static-1 hazard with suitable example.

Or

(b) Explain how hazards can be represented using a K-map.

(4 × 10 = 40 marks)