APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

Q. P. code : 3BC-16-1 **(pages: 2)** **Name:**

Reg No:

THIRD SEMESTER M.TECH. DEGREE EXAMINATION DEC 2016

Computer Science and Engineering

08 CS 7021(C): ADVANCED ARCHITECTURE

Time:3 hours **Max. Marks: 60**

Answer all six questions. Part 'a' of each question is compulsory.

Answer either part 'b' or part 'c' of each question

Q.no.	Module 1	Marks
1.a	Draw the block diagram of a micro-coded control unit and explain its function.	3
	Answer b or c	
b	Develop the micro code for add instruction.	6
c	Write the control sequences for 1 bus and 2 bus SRC add instruction. Obtain the speed up obtained in 3 bus architecture over 1 bus architecture.	6

Q.no.	Module 2	Marks
2.a	What is multi-processor cache coherence?	3
	Answer b or c	
b	Explain how multi-level caches are organized in a multi-processor shared architecture. Also explain the inclusion property. Explain the chances of not satisfying the inclusion property.	6
c	Explain the modified, exclusive and shared invalid state diagram of cache coherence protocols.	6

Q.no.	Module 3	Marks
3.a	Based on the following program segments and on the assumption that the processes are running on two different processors with X and Y originally cached with initial value 0, explain the possible memory inconsistency. Suggest a suitable consistency model. What is relaxed consistency?	3

P1 :	X =0	P1 :	Y =0
	.....		.....
	X=1		Y=1
	If (Y==0)		If (Y==0) ....

Answer b or c

b	Explain how synchronisation is achieved using basic hardware primitives.	**6**
c	The following instructions are executed using Tomasulos Algorithm. Explain the implementation of Tomasulos Algorithm and show the instruction status, reservation station and register result status at clock no 12. Assume, 3 Add R S units, 3 Load R S units and 2 Mult R S units are available. ADD takes 2 clock cycle, MULT takes 6 clock cycles and DIV takes 12 clock cycles for execution L.D F6, 34(R2) L.D F2, 45(R3) DIV.D F6, F6, F2 ADD.D F10, F4, F6. MUL.D F8, F4, F2 SUB.D F4, F6, F2	**6**

Q.no.	**Module 4**	**Marks**
4.a	What are homogeneous and heterogeneous cores?	**3**
	Answer b or c	
b	Discuss how resource sharing is done in multi core processors.	**6**
c	Explain a typical multicore architecture with advanced pipelining and memory system components.	**6**

Q.no.	**Module 5**	**Marks**
5.a	Briefly explain granularity and load balancing.	**4**
	Answer b or c	
b	Explain the possible variations of multi-threading in multi-core architecture.	**8**
c	Develop a multi-threaded algorithm for matrix multiplication. Analyse the performance and compare it with sequential implementation.	**8**

Q.no.	**Module 6**	**Marks**
6.a	With the help of suitable examples, explain work sharing in OpenMP.	**4**
	Answer b or c	
b	(i) Explain with suitable examples how critical section can be implemented in OpenMP. (ii)With the help of suitable examples, explain the following features of OpenMP. a) Critical b) atomic c) barrier d) reduction	**8**
c	Write an OpenMP program to compute Fibonacci number. Use task directive in the function fib(n) . Explain the concept of task directive used in the program.	**8**