APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

SECOND SEMESTER M.TECH DEGREE EXAMINATION, MAY 2016

Computer Science and Engineering

08 CS 6012 Advanced Compiler Design

Max. Marks : 60 Duration : 3 Hours

Answer ALL six questions. Part (a) of each question is compulsory.

Answer EITHER part (b) *or* part (c) of each question.

Q.No. Marks

Module I

1a. Differentiate between Inherited and Synthesized Attributes. 3

Answer b *or* c

b. Given the Syntax-Directed Definition below with the synthesized attribute val, draw the annotated parse tree for the expression (3+4) * (5+6).

$L \rightarrow E$	L.val = E.val
$E \rightarrow T$	E.val = T.val
$E \rightarrow E1 + T$	E.val = E1.val + T.val
$T \rightarrow F$	T.val = F.val
$T \rightarrow T1 * F$	T.val = T1.val * F.val
$F \rightarrow (E)$	F.val = E.val
$F \rightarrow$ digit	F.val = digit.lexval

6

c. What are Syntax-Directed Translations? Explain the Parser Stack implementation of Postfix Syntax-Directed Translations. 6

Module II

2.a Create a Three-address code and its quadruple representation for the assignment

a = b * - c + b * - c 3

Answer b *or* c

2b. Justify the statement: Back patching can be used to generate code for Boolean expressions and flow-of-control statements in one pass.

6

c.Write the syntax of Switch statement .Explain Syntax Directed Translation of Switch Statements. 6

Module III

3a.Briefly describe the performance metrics considered while designing garbage collector? 3

Answer b *or* c

b.What is an Activation tree? Discuss the significance of activation tree and activation records in Compiler 6

c. Discuss the role of memory manager in Heap management? List out the most popular conventions and tools used for managing memory. 6

Module IV

4a. What is a Directed Acyclic graph? Draw the Directed Acyclic graph for the following:-

```
t0 = a+b
t1 = t0+c
d = t0+t1
```

3

Answer b *or* c

b.Explain algorithm for Partitioning Three-address Instructions into Basic Blocks.Draw the flow graph representation for the given intermediate code.

```
1.  i = 1
2.  j = 1
3.  t1 = 10 * i
4.  t2 = t1 + j
5.  j = j + 1
6.  if j <= 10 goto (3)
7.  i = i + 1
8.  if i <= 10 goto (2)
9.  i = 1
10. t3 = i – 1
11. if i <= 10 goto (10)
```

6

c. Describe Instruction selection by Tree Rewriting considering all the issues associated with code generation by Tiling an Input tree? 6

Module V

5a. Define code optimisation. List the Criteria for Code-Improving Transformations. 4

Answer b *or* c

b.Consider the example of quick sort to demonstrate the principal sources of Optimization? Draw a flow graph for the three address code for the quicksort fragment? **8**

c . Briefly explain the constraints in Data flow Analysis Schema? With the help of Iterative algorithm discuss Reaching definitions? **8**

Module VI

6a.Discuss the factors that depend on how fast can a program run on a processor with instruction parallelism. **4**

Answer b *or* c

b.(i) Explain Global Code Scheduling. Illustrate the steps to be considered while creating a globally scheduled machine code for the source code . **5**

(ii)Differentiate upward Code Motion and Downward code motion. **3**

c. Analyse the code scheduling constraints in program optimisation considering the trade-off between register usage and parallelism. **8**