C 1040 (Pages : 2) Name.....

Reg. No.....

EIGHTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, APRIL 2016

CS 09 801—COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. How to calculate the cost of integrated circuits ?
2. What is thread level parallelism ?
3. What is the use of virtual memory ?
4. What is the role of multiprocessing in microprocessor architecture ?
5. What are the different levels of branch prediction ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Explain data hazards in detail.
7. Explain compiler vectorization.
8. Explain the performance of Unix file system.
9. Describe centralized memory architecture.
10. How to encode an instruction set ?
11. Explain the protection and working of virtual memory.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) Define the terms 'structural hazard', 'control hazard', and 'data hazard' in the context of pipelines. Which of these hazards is addressed by a hardware branch prediction ?

Or

(b) With neat diagram explain instruction set architecture.

Turn over

13. (a) Explain how parallelism is achieved in uniprocessor systems.

Or

(b) Explain vector processing in detail.

14. (a) With neat diagram explain memory hierarchy design in detail.

Or

(b) Describe the use of bench mark. Explain various types of bench marks in detail.

15. (a) With a neat diagram explain cache coherence in a distributed shared memory multiprocessor.

Or

(b) Briefly explain shared memory architecture in detail.

(4 × 10 = 40 marks)