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Name..

Reg. No.

# SIXTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, APRIL 2016

EC/PTEC 09 601—VLSI DESIGN

Time: Three Hours

Maximum: 70 Marks

#### Part A

# Answer all the questions

- 1 What are the factors that cause static power dissipation in CMOS circuits?
- 2 Give the effect of supply voltage and temperature variations on the CMOS system performance.
- 3 Distinguish between depletion mode and enhancement mode MOSFET.
- 4 What is a contrast curve? Give its significance in VLSI fabrication.
- 5 Define the lambda layout rules.

 $(5 \times 2 = 10 \text{ marks})$ 

#### Part B

## Answer any four questions

- 6 Explain different types of technology scaling. Illustrate the impact of full scaling on Drain current, Gate capacitance and power delay product.
- 7 Explain Pseudo NMOS logic.
- 8 Explain the operation of a SRAM with neat sketch.
- 9 Explain Oxidation.
- 10 Explain twin tub process.
- 11 Draw the circuit schematic and stick diagram of CMOS 2 input NAND gate.

 $(4 \times 5 = 20 \text{ marks})$ 

#### Part C

### Answer all questions

12 (a) Explain the operation of a CMOS inverter and derive an expression for its propagation delay.

Or

(b) Explain the transfer plot of CMOS inverter with necessary expression for  $V_{\rm out}$  in each region.

Turn over

- 18 (a) How to read or write and hold the bit in SRAM cell?
  - (b) Explain the working of 1-transistor DRAM cell. Give the difference between SRAM and DRAM.
- 14 (a) What is Oxide masking? Explain how impurity redistribution takes place during oxide growth.

Or

- (b) Explain the constant source diffusion and the limited source diffusion process.
- 15 (a) Explain LOCOS, SILO and SWAMI process.

Or

(b) Describe in detail step-by-step procedure of P-well CMOS fabrication.

 $(4 \times 10 = 40 \text{ marks})$ 

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