C 1138 (Pages : 2) Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, APRIL 2016

AI 09 L03—DIGITAL DESIGN WITH VHDL

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. What are the Arithmetic operators defined in VHDL ?
2. Give an example for Physical literals used in VHDL. Mention its usage.
3. Differentiate between array and record.
4. What is positional mapping ?
5. What do you mean by D'LAST_ACTIVE attribute ? (Assume D is a signal).

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Write notes on Enumerated data types.
7. Obtain the VHDL model for a full adder circuit.
8. Compare signals and Variables.
9. Write a VHDL code to implement a latch with asynchronous reset using CASE statement.
10. Write a VHDL code to model a D flip-flop. A function "positive_edge()" is used to sample the data inputs.

    (Write the VHDL code for the function "positive_edge()" and locate in a package).
11. Describe the commonly occurring faults in combinational logic with examples.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) Obtain the VHDL model for a 3 to 8 decoder.

Or

(b) (i) Compare the CASE and WHEN statements in VHDL. (5 marks)

(ii) Implement 2 × 1 MUX using IF. (5 marks)

Turn over

13. (a) Write notes on : (i) ASSERT statement ; (ii) Procedures.

Or

(b) Design a non-overlapping sequence detector to detect "01011" in VHDL.

14. (a) Design a stop watch in VHDL with an n bit counter and an n bit register as components.

(Assume a stop control in the ckt . When stop = 1 counter goes to reset mode and the status of counter is stored in the register. When stop = 0 counter resumes counting.).

Or

(b) Design a 4 bit array multiplier in VHDL with full adder and half adder circuits defined as components in a package.

15. (a) Explain Scan testing with appropriate example.

Or

(b) Write notes on : (i) Built in self test ; (ii) Signal attributes.

(4 × 10 = 40 marks)