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Name.....................

Reg. No.....................

SIXTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, APRIL 2016

AI 09 601 – DIGITAL SIGNAL PROCESSING

Time : Three Hours

Maximum : 70 Marks

Part A

Answer **all** *questions.*

I. 1. State the differences between decimation in time and frequency in time FFT algorithms.

2. Find the DTFT of $3^n u(n)$?

3. What is a signal flow graph?

4. Draw the frequency response curves of LPF and BSF.

5. Write two features of TMS 320 series processor.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

II. 1. Explain the decimation in time algorithm.

2. State and prove any *three* properties of DFT.

3. Draw the direct form II structure of $H(2) = \dfrac{3z^3 - 5z^2 + 9z - 3}{\left[z - \frac{1}{2}(z^2 - z + \frac{1}{3})\right]}$.

4. Find the lowest order of Chebysher filter that meets the following specifications :

   (i) 1 dB ripple in the passband $0 \le |w| \le 0.3\bar{\Lambda}$.

   (ii) Atleast 60 dB attenuation in the stopband $0.35\bar{\Lambda} \le |w| \le \bar{\Lambda}$.

   Use bilinear transformation.

5. Discuss the properties of Butterworth filter.

6. Explain briefly the Harvard computer architecture.

(4 × 5 = 20 marks)

Turn over

Part C

Answer **all** *questions.*

III. (a) Perform the linear convolution of the sequences { 1, –2, 3, 2, –3, 4, 3, –4} and {1, 2, –1} using overlap-save method.

Or

(b) Find the IDFT of the sequence $X(k) = \{4, 1 - j\,2.414, 0, 1 - j\,0.414, 0, 1 + j\,0.414, 0, 1 + j\,2.414\}$ using DIF algorithm.

IV. (a) Obtain the cascade and parallel forms of the system described by :

$$y(n) = -\frac{13}{13}\, y(n-1) - \frac{19}{24}\, y(n-2) - \frac{5}{24}\, y(n-3) + x(n) + 4x(n-1) + 3\,x(n-2).$$

Or

(b) Explain about limit cycle oscillations and scaling of overflow protection in digital systems.

V. (a) Design a low-pass Butterworth digital filter to give response fo 3 dB or less for frequencies upto 2 kHz and an attenuation of 20 dB or more beyond 4 kHz. Use bilinear transformation and obtain H (*z*) of the desired filter.

Or

(b) (i) Explain impulse invariant method of digital filter design.

(ii) Convert the analog filter $H_a(s) = \dfrac{2}{(s+0.4)^2 + 4}$ into a digital filter using impulse invariant transformation.

(5 + 5 = 10 marks)

V. (a) Explain the structure of a :

(i) General purpose DSP processor.

(ii) Discuss any *two* special instructions of DSP.

(6 + 4 = 10 marks)

Or

(b) Write notes on special purpose :

(i) DSP hardware.

(ii) Discuss a concept of implementing a multiplier.

(7 + 3 = 10 marks)

[4 × 10 = 40 marks]