D 90006 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) [14 SCHEME] DEGREE EXAMINATION, NOVEMBER 2015

CS/IT 14 306—SWITCHING THEORY AND LOGIC DESIGN

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **eight** *questions.*

1. Prove : $X.Y + X'.Z + Y.Z = X.Y + X'.Z$.
2. Simplify the following expression using Boolean Algebra :–

   (i) $(A\,B + A\,(C\,D + C\,D')$

   (ii) $(B\,C' + A'\,D)\,(A\,B' + C\,D')$

3. Design a 8 to 3 encoder with proper diagram and logic diagram.
4. Implement a Boolean expression $F(A, B, C) = \sum m(1, 2, 6, 7)$ using approximate Multiplexers.
5. Write short notes about ripple counters.
6. List the applications of Flip-flops.
7. Write notes on Fault diagnosis and tolerance.
8. Describe the fault classes models in detail.
9. Explain with example how don't care conditions are implemented in K map minimization.
10. Write notes on EPROM and EEPROM.

(8 × 5 = 40 marks)

Part B

11. Explain the following with suitable example :

    (a) Quine McClusky Algorithm.

    (b) Generalization of DeMorgan's laws.

Or

12. Discuss in detail about switching expressions with suitable examples.
13. Design the carry look ahead adder for a 4 bit binary number.

Or

Turn over

14. What is a data selector ? Design a 16 : 1 MUX using 4 : 1 MUX with relevant diagrams and explanations.

15. Explain with neat diagrams and tables about different Flip-flops.

Or

16. Explain excitation table for the various types of Flip flops.

17. Explain the different fault tolerance techniques in detail.

Or

18. Write detailed notes on Fault diagnosis and testing.

(4 × 15 = 60 marks)