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(Pages : 2)

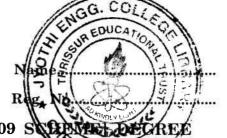# FIFTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, NOVEMBER 2015

EC/PTEC 09 506—LINEAR INTEGRATED CIRCUITS

Time : Three Hours   Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. What is the significance of level shifting stage in an operational amplifier circuit ?

2. The slew rate of op-amp 1 V/μs. How it can be explained by showing square wave input and output waveform ?

3. Draw the attenuation slope of a first order and second order high-pass active filter. Compare its performance.

4. Draw the circuit diagram of a R-2R DAC using op-amp. Why it is called 'R-2R' ?

5. What do you mean by free running frequency in PLL ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

1. Draw the circuit diagram of a summing circuit with following input-output relationship,

$V_o = V_{i1} + V_{i2} - (V_{i3} + V_{i4})$.

2. Draw a Schmitt trigger circuit using op-amp and explain its working. Design the circuit for UTP = + 3V and LTP = –2V.

3. Explain the operation of RC phase-shift oscillator using op-amp. What is the gain of the op-amp circuit and significance of 3 RC networks.

4. Draw the internal diagram of 555 IC and the operation as astable multivibrator using this chip.

5. Draw the circuit of adjustable voltage regulator and explain how variable voltage is obtained at the output.

6. Draw the basic block diagram of Phase Locked Loop and explain each block.

(4 × 5 = 20 marks)

Turn over

Part C

Answer **all** *questions.*

1. Draw the detailed internal diagram of op-amp and explain each block with simplified circuit diagram.

(5 + 5 = 10 marks)

Or

2. Draw and explain an instrumentation amplifier circuit using 3 op-amps. Derive the expression for final gain of the above circuit.

(6 + 4 = 10 marks)

3. Design a monostable multivibrator circuit using op-amp with given specifications : $V_{cc} = \pm 15V$, Input trigger signal: 5V, 1 kHz square pulse, Duty cycle: 70 %. Draw input-output waveforms.

(7 + 3 = 10 marks)

Or

4. Explain and draw a second order low-pass butterworth filter using op-amp :

    (a) Obtain the expression for high cut-off frequency f_H and gain A_F.

    (b) Draw its frequency response showing f_H.

(5 + 3 + 2 = 10 marks)

5. Draw and explain DAC using binary weighted resistors. Show the graph showing input-output relations and explain the resolution of the output.

(5 + 3 + 2 = 10 marks)

Or

6. Draw the circuit diagram of a ramp generator using 555 IC with necessary waveforms showing time periods and voltage levels. Explain its working in detail.

(6 + 4 = 10 marks)

7. Draw the internal block diagram of 565 PLL IC and explain the working of each block. Explain the capture range and lock range of PLL and show them in a band spectrum.

(6 + 4 = 10 marks)

Or

8. Draw the detailed diagram of frequency multiplier ($f_{out} = 2\,f_{in}$) using PLL and explain its working.

(6 + 4 = 10 marks)

[4 × 10 = 40 marks]

Part C

Answer **all** *questions.*

1. Draw the detailed internal diagram of op-amp and explain each block with simplified circuit diagram.

(5 + 5 = 10 marks)

Or

2. Draw and explain an instrumentation amplifier circuit using 3 op-amps. Derive the expression for final gain of the above circuit.

(6 + 4 = 10 marks)

3. Design a monostable multivibrator circuit using op-amp with given specifications : $V_{cc} = \pm 15V$, Input trigger signal: 5V, 1 kHz square pulse, Duty cycle: 70 %. Draw input-output waveforms.

(7 + 3 = 10 marks)

Or

4. Explain and draw a second order low-pass butterworth filter using op-amp :

    (a) Obtain the expression for high cut-off frequency f_H and gain A_F.

    (b) Draw its frequency response showing f_H.

(5 + 3 + 2 = 10 marks)

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[4 × 10 = 40 marks]