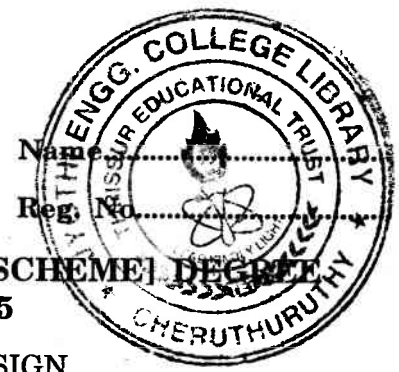


**D 90152**

(Pages 2)



**FIFTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE  
EXAMINATION, NOVEMBER 2015**

**EE/PT EE 09 505—DIGITAL SYSTEM DESIGN**

Time : Three Hours

Maximum : 70 Marks

**Part A**

*Answer all questions.*

1. Write the structure of VHDL program.
2. Give two guidelines for state assignment.
3. Differentiate between Moore and Mealy machine.
4. Write the VHDL for a 2-bit multiplexer.
5. What is a primitive flow table ?

(5 × 2 = 10 marks)

**Part B**

*Answer any four questions.*

6. Explain briefly about entity and its function.
7. Write the VHDL program for a 4 to 2 decoder.
8. Give the excitation table for JK flip-flop and D flip-flop along with their characteristic equations.
9. Differentiate between functions and procedures in VHDL.
10. What do you understand by race-free state assignment ?
11. Write short note on Instate and bistate devices.

(4 × 5 = 20 marks)

**Part C**

*Answer all questions.*

12. (a) Discuss the features of libraries and packages in VHDL with example.  
*Or*  
(b) With suitable examples discuss the various behavioural design elements.
13. (a) Write a VHDL program for 8 to 1 mux and use it as a component for realisation of 64 to 1 mux.

*Or*

- (b) Using VHDL write the code to perform 3-bit addition and subtraction with Behavioural and structural description.

**Turn over**

14. (a) Design a synchronous sequential circuit that functions as a sequence detector to detect a sequence of 1011 using D flip-flop.

*Or*

- (b) With a suitable example design a synchronous circuit, its state table, equation and diagram.
15. (a) What are the components and salient features of the ASM chart ? Explain with suitable examples where necessary.

*Or*

- (b) Explain the architecture of XC FPGA CLB.

(4 × 10 = 40 marks)