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Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. [ENGINEERING] (09 SCHEME) DEGREE EXAMINATION, NOVEMBER 2015

EC/PTEC 09 703—ANALOG AND MIXED MOS CIRCUITS

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. List out the limitations of CMOS technology.
2. Mention the advantages of cascode amplifiers.
3. What is a Miller effect ?
4. What is meant by PSRR ?
5. Define hysteresis.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Explain how could a MOS transistor act as a switch.
7. Discuss the operation of breakdown-diode voltage reference circuit.
8. Explain the noise model of a differential amplifier.
9. Discuss the characterization of operational amplifier circuits.
10. Explain the operation of folded cascode opamp circuits.
11. Describe the working principle of basic comparator.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) (i) Derive R_{out} and V_{min} for the Wilson current mirror circuit using small signal model analysis. (6 marks)

(ii) Discuss the non-ideal effects of current mirror circuit. (4 marks)

Or

(b) Discuss the behaviour of large signal model for *n*-channel MOS transistor.

Turn over

13. (a) Discuss the large signal and small signal analysis of a differential amplifier.

Or

(b) Explain the working principles of single-ended and differential input current amplifier circuits.

14. (a) Explain the complete design procedure of two-stage CMOS operational amplifier with necessary equations.

Or

(b) Explain the operation of switched capacitor amplifiers with proper circuit diagrams.

15. (a) (i) Discuss the non-ideal effects in PLL. (6 marks)

(ii) Explain the significance of loop filter in PLL. (4 marks)

Or

(b) Write short notes on :

(i) Analog Multiplier. (5 marks)

(ii) Sample and Hold circuits. (5 marks)

[4 × 10 = 40 marks]