C 80755 (Pages : 2)

Name .....

Reg. No. .....

SIXTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, APRIL 2015

EC/PTEC 09 601—VLSI DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Define Power dissipation.
2. Define scaling. Mention the types of scaling.
3. What is the need for testing ?
4. Write down the equation for describing the channel length modulation effect in NMOS transistors.
5. What is the objective of layout rules ?

(5 × 2 = 10 marks)

Part B

6. Write a note on MOS models.
7. How to avoid unequal delays in NMOS logic circuits.
8. Explain the working of 3T DRAM.
9. Draw the layout of 2 input NMOS nor gate.
10. Draw V-I characteristics of a NMOSFET in the enhancement mode and mark the regions of operation.
11. Consider the design of a 16-input AND gate in static CMOS explain why the 2-input design could not simply be scaled up.

(4 × 5 = 20 marks)

Part C

12. (a) Explain the DC characteristics of CMOS inverter with neat sketch.

Or

(b) Explain the different regions of operation in a MOS transistor.

13. (a) Write the verilog code for 4 bit ripple carry full adder.

Or

(b) Design a full adder circuit using : (i) NMOS switches; and (ii) CMOS switches. Using the adder as a block, design a 4 bit ALU and illustrate the operation.

Turn over

14. (a) Draw V-I characteristics of a NMOSFET in the enhancement mode and mark the regions of operation. Indicate how the V-I curve gets modified if (i) We increase the width of transistor; (ii) We consider velocity saturation; (iii) We consider Channel Length Modulation.

Or

(b) Explain channel length modulation and body effect.

15. (a) Briefly discuss about the CMOS process enhancements and layout design.

Or

(b) Discuss the need for testing and explain about the silicon debugging principles.

(4 × 10 = 40 marks)