C 80692 (Pages : 2) Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE (09 SCHEME) EXAMINATION, APRIL 2015

EC 09 405/PTEC 09 404—COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*
Each question carries 2 *marks.*

1. What do you mean by bus ?
2. What is cache memory ?
3. What is content addressable memory and what are advantages of this memory ?
4. What is DMA ?
5. What is microinstruction and microprogram ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

6. List and explain the computer system components ?
7. Explain direct, indirect, immediate and register addressing modes using examples and illustrations.
8. Explain how the multiprocessors are classified based on way their memory organization.
9. Draw and explain the block diagram of a complete processor.
10. Explain how data transfer takes place between an I/O device and processor in a program controlled I/O.
11. Explain how multiple simultaneous interrupt request is handled by processor.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (A) Draw bus interconnection scheme and explain the function of each bus.

Or

(B) What do you mean by interconnection structures ? Draw interconnection structures for memory, input/output and CPU modules.

Turn over

13. (A) What is cache memory ? Explain different mapping techniques used in the usage of cache memory.

Or

(B) Explain approaches for addressing multiple- module memory systems with suitable diagrams.

14. (A) Explain the working of DMA ? Also mention its advantages.

Or

(B) What is the function of a multiprocessor system and list out the various characteristics of multiprocessor ?

15. (A) Describe the hardware mechanism for handling multiple interrupt requests.

Or

(B) What are handshaking signals? Explain the handshake control of data transfer during input and output operation.

(4 × 10 = 40 marks)