C 80690 (Pages : 2) Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (09 SCHEME) (ENGINEERING) DEGREE EXAMINATION, APRIL 2015

EC 09 403/PTEC 09 402—ELECTRONIC CIRCUITS

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*
Each question carries 2 *marks.*

I. 1 What is current foldback scheme ?

2 What is the need for Darlington pair in power amplifier ?

3 Define CMRR.

4 How non-saturating switches are designed ?

5 Where electrolytic capacitors are used ? Why ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

II. 1 How variable resistors are designed ? Explain.

2 Derive the expression for rectification efficiency of a full wave rectifier.

3 For a class B amplifier operating at a supply voltage of 20 V and driving a load resistance of 10 Ω, calculate the maximum input power, output power and transistor dissipation.

4 Explain the DC load line of a BJT amplifier.

5 Explain the frequency response of an emitter follower.

6 Explain the operation of BJT as a switch.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*
Each question carries 10 *marks.*

III. 1 Derive the parameters of hybrid π model of BJT.

Or

2 Compare and contrast the CC, CB and CE configurations.

Turn over

IV. 3 Describe the configurations of feedback amplifiers.

Or

4 Discuss the working of class AB and class D power amplifier.

V. 5 Discuss the construction and VI characteristics of JFET.

Or

6 Describe the characteristics of UJT and differential amplifier.

VI. 7 Explain the operation of self biased transistor bistable circuit.

Or

8 Explain the operation of collector coupled multivibrator circuit.

(4 × 10 = 40 marks)