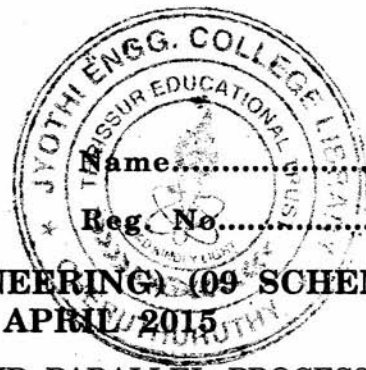


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**EIGHTH SEMESTER B.TECH. (ENGINEERING) (09 SCHEME)  
DEGREE EXAMINATION, APRIL 2015**

**CS 09 801—COMPUTER ARCHITECTURE AND PARALLEL PROCESSING**

Time : Three Hours

Maximum : 70 Marks

**Part A**

*Answer all questions.*

1. State few performance measurements of a typical computer design.
2. Define instruction level parallelism.
3. What do you mean by miss penalty ?
4. Write about the practical issues faced in connecting more than two computers.
5. What is the use of an instruction set ?

(5 × 2 = 10 marks)

**Part B**

*Answer any four questions.*

6. Distinguish between data hazard and control hazard.
7. State few quantitative principles of computer design and explain with an example.
8. How to enhance vector performance ? Give an example.
9. Brief about memory hierarchy design.
10. Explain in detail about centralized shared memory.
11. Discuss about the main memory and virtual memory.

(4 × 5 = 20 marks)

**Part C**

*Answer all questions.*

12. (a) Explain in detail about encoding an instruction set.  
*Or*  
(b) Define pipelining. Explain in detail about pipeline for DLX.
13. (a) What is dynamic scheduling ? Explain in detail about hardware support for ILP.  
*Or*  
(b) Write about vector architecture and compiler vectorization.

**Turn over**

14. (a) Explain in detail about protection mechanism involved in the Intel pentium processor.

*Or*

(b) Explain about I/O performance measures.

15. (a) Discuss about the practical issues in connecting two computers.

*Or*

(b) With neat sketches write about models of memory consistency.

(4 × 10 = 40 marks)