D 70194 (Pages : 2) Name.....

Reg. No.....



# SEVENTH SEMESTER B.TECH. (ENGINEERING) (09 SCHEME) DEGREE EXAMINATION, NOVEMBER 2014

## EE/PTEE 09 703—DIGITAL SIGNAL PROCESSING

Time : Three Hours Maximum : 70 Marks

### Part A

*Answer* **all** *the questions.*
*Each question carries* 2 *marks.*

1. What is the difference between DFT and Z-transform ?
2. Define ROC.
3. Compare the cascade and Parallel form of filter structures.
4. What is Gibbs Phenomenon ?
5. Compare Fixed point and Floating point arithmetic.

(5 × 2 = 10 marks)

### Part B

*Answer any* **four** *questions.*
*Each question carries* 5 *marks.*

6. Find DFT of the sequence $x(n) = \{1, 1, 1, 0\}$ using DIT algorithm.
7. Explain in detail about Direct form realization of FIR filters.
8. Write short notes on direct form to lattice structure.
9. Design an ideal band pass filter with frequency response.

   $H_d(e^{jw}) = 1$ for $\pi/4 \leq |w| \leq 3\pi/4$

   $= 0$ otherwise

   Find the value of $h(n)$ for N = 7.
10. Write short notes on zero input limit cycle oscillations.
11. Explain any *two* application of DSP processor.

(4 × 5 = 20 marks)

Turn over

## Part C

*Answer* **all** *questions.*

12. (a) Compute the eight — point DFT of the sequence $x(n) = \{1, 1, 1, 1, 0, 0, 1, 1\}$ using the in place radix-2 DIF algorithm

*Or*

(b) Explain in detail about overlap save method of convolution.

13. (a) Realize the system given by difference equation.

$$y(n) = -0.1\,y(n-1) + 0.72\,y(n-2) + 0.7\,x(n) - 0.252\,x(n-2)$$ in parallel form.

(b) An FIR filter is given by the difference equation

$$y(n) = 2\,x(n) + 4/5\,x(n-1) + 3/2\,x(n-2) + 2/3\,x(n-3).$$

14. (a) Design a Fourth order Butterworth digital filter using bilinear transformation technique. Assume sampling period T = 2 sec.

*Or*

(b) Write the design steps FIR filters using windowing technique.

15. (a) Consider the transfer function $H(z) = H_1(z)\,H_2(z)$ where

$$H_1(z) = \frac{1}{1 - a_1 z^{-1}} \text{ and } H_2(z) = \frac{1}{1 - a_z z^{-1}}$$

Assume $a1 = 0.5$ and $a2 = 0.6$ and find the output round-off noise power.

*Or*

(b) Explain the architecture of TM320 C67X DSP Processor.

(4 × 10 = 40 marks)