D 70295 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) (09 SCHEME) DEGREE EXAMINATION, NOVEMBER 2014

EE/PTEE 09 505—DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *the questions.*
Each question carries 2 *marks.*

1. Write the VHDL code for a 2 input XOR gate.
2. List the entity elements in VHDL.
3. What are tristate devices ?
4. Give the guidelines for state reduction.
5. What are the blocks involved in ASM charts ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*
Each question carries 5 *marks.*

6. List out the essential features of VHDL language.
7. Differentiate between functions and procedures in VHDL.
8. Briefly explain the rules to perform bubble-to-bubble logic.
9. Give the excitation table for JK flip-flop and D flip-flop along with their characteristic equations.
10. What are pipelined output ?
11. Draw the ASM chart for MOD-5 counter.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) With suitable example discuss the various data flow design elements.

Or

(b) Explain in detail about types, constants and arrays.

Turn over

13. (a) Write the VHDL code to realize a 4-bit magnitude comparator.

Or

(b) Discuss the salient features of circuit timing and timing specification.

14. (a) Design a synchronous sequential circuit that functions as a sequence detector to detect a sequence of 0110 using JK flip-flop.

Or

(b) Design a sequential circuit with two DFFs A and B, and one input x. When $x = 0$ the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transition from 00 to 01 to 11 to 10 and back to 00 and repeats.

15. (a) Discuss the analysis of circuits with multiple feedback loops with examples.

Or

(b) Explain in detail about races with state table and flow table.

(4 × 10 = 40 marks)