**D 70383**

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**Name.........................................**

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# THIRD SEMESTER B.TECH. (ENGINEERING) (09 SCHEME) DEGREE EXAMINATION, NOVEMBER 2014

EC 09 305/PT EC 09 304—DIGITAL ELECTRONICS

Time : Three Hours

Maximum : 70 Marks

## Part A

*Answer* **all** *questions.*

1. State De-Morgan's theorem.
2. Simplify the given Boolean expression $F = \overline{x} + xy + x\overline{z} + x\overline{yz}$.
3. Convert the hexadecimal number $(A25F)_{16}$ into a decimal number.
4. How many flip-flops are required to construct a binary counter that counts from 0 to 1023 ?
5. Compare the ASM chart with a conventional flow chart.

(5 × 2 = 10 marks)

## Part B

*Answer any* **four** *questions.*

6. Realize the given boolean expression $Z = ABC + AD + \overline{CD}$ using only two-input NAND gates. Use as few gates as possible.
7. Compare the performance of ECL and TTL logic.
8. Draw the logic diagram of BCD adder and explain its operation.
9. Convert D-Flip-flop into JK-flip-flop.
10. Discuss the various triggering methods used in flip-flops.
11. Explain the various building blocks in ASM chart.

(4 × 5 = 20 marks)

## Part C

*Answer* **all** *questions.*

12. (a) Minimize the given switching function using Quine-McCluskey method.

$$F(A, B, C, D) = \Sigma(0, 5, 7, 8, 9, 10, 11, 14, 15).$$

*Or*

**Turn over**

(b) (i) Express the Boolean function F = XY + XZ in product of maxterms. (4 marks)

(ii) Reduce the following function using K-map technique :

$f(A, B, C, D) = \pi(0, 3, 4, 7, 8, 10, 12, 14) + d(2, 6)$. (6 marks)

13. (a) Design a four bit BCD to excess-3code converter. Draw logic diagram for the same.

*Or*

(b) (i) Implement the following function using a suitable multiplexer.

$F(A,B,C,D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$ (6 marks)

(ii) Design a full adder circuit using two half adders and an OR gate. (4 marks)

14. (a) (i) Design a 4-bit bidirectional shift register with neat logic diagram. (5 marks)

(ii) Design a 3-bit Johnson counter and explain its operation. (5 marks)

*Or*

(b) Explain in detail the operation of a 4-bit binary ripple counter.

15. (a) Design a sequence detector which detects the sequence "01110" using D flip-flops (one bit overlapping).

*Or*

(b) Design a sequential circuit that has two inputs, $w_1$ and $w_2$ and an output, z. Its function is to compare the input sequences on the two inputs. If $w_1 = w_2$ during any four consecutive clock cycles, the circuit produces z = 1 ; otherwise, z = 0. For an example,

| | | |
|---|---|---|
| $w_1$ | ... | 0110111000110 |
| $w_2$ | ... | 1110101000111 |
| z | ... | 0000100001110 |

(4 × 10 = 40 marks)