D 70181 (Pages : 2) Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, NOVEMBER 2014

EC/PTEC 09 703 – ANALOG AND MIXED MOS CIRCUITS

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

1. Define the terms : Current sink and Current source.
2. What do you mean by parasitic resistance and capacitance?
3. What is a miller effect?
4. Give the significance of slew rate in an operational amplifier.
5. Mention the advantages and disadvantages of ladder approach in designing switched capacitor filter.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Derive R_{out} and V_{min} for the Wilson current mirror circuit using small signal model analysis.
7. Analyze the noise performance of the common source amplifier.
8. Explain the working of CMOS differential amplifier using current mirror as an active load.
9. Discuss the frequency compensation techniques for single stage CMOS operational amplifier.
10. Explain the working of any *one* type of the comparator circuit.
11. Discuss the significance of sample and hold circuit.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

12. (a) Describe how could the high performance voltage reference be obtained using various elements.

Or

(b) (i) Explain how could a MOS transistor act as a switch.

(ii) Discuss the behaviour of sub threshold MOS transistor model.

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13. (a) How is cascode amplifier better than an inverting amplifier? Derive the frequency response of the cascode amplifier circuit.

Or

(b) Discuss the various architectures proposed to design a high gain amplifier.

14. (a) Explain the working of switched capacitor amplifier and integrator with a neat circuit.

Or

(b) What are the advantages of cascode op-amps? Discuss the use of cascoding in first stage and second stage of an op-amp with suitable circuit diagrams.

15. (a) (i) Explain the working of a simple charge pump Phase Locked Loop (PLL).

(ii) Discuss the non-ideal effects in PLL.

Or

(b) (i) Describe the operation of voltage controlled oscillator using source coupled CMOS configuration.

(ii) Discuss the significance of the analog multiplier circuit.

(6 + 4 = 10 marks)

[4 × 10 = 40 marks]