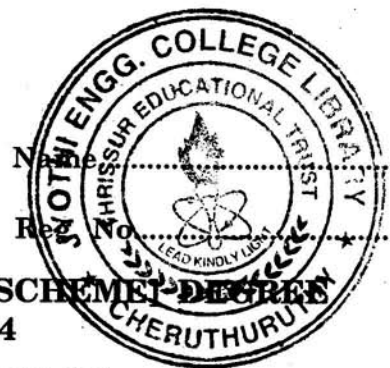


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**FIFTH SEMESTER B.TECH. (ENGINEERING) [09 SCHEMEL-DEGREE]
EXAMINATION, NOVEMBER 2014**

EC/PTEC 09 501—DIGITAL SIGNAL PROCESSING

Time : Three Hours

Maximum : 70 Marks

Part A

*Answer all the questions.
Each question carries 2 marks.*

1. Write the Symmetry property of Discrete Fourier Series.
2. Write the Linearity Property of DFT.
3. What are source nodes in signal flow graph ?
4. Write the Hanning Window functions.
5. How is execution of Program done in the DSP Processor ?

(5 × 2 = 10 marks)

Part B

*Answer any four questions.
Each question carries 5 marks.*

1. Find the N-point DFT for $x(n) = a^n$ for $0 < a < 1$.
2. Explain overlap-save method with example.
3. Draw the cascade realization of :

$$H(z) = \frac{(1 - z^{-1})^3}{\left(1 - \frac{1}{2}z^{-1}\right)\left(1 - \frac{1}{8}z^{-1}\right)}$$

4. Explain round-off error for sign magnitude and two's Complement representation.
5. Convert the analog filter with system function $H(s) = \frac{s + 0.1}{(s + 0.1)^2 + 9}$ into digital IIR filter using

bilinear transformation. The digital filter should have a resonant frequency of $\omega_r = \frac{\pi}{4}$.

6. Explain 1st design iteration in FFT Processor.

(4 × 5 = 20 marks)

Turn over

Part C

Answer all questions.

1. Explain radix-2 decimetric in frequency FFT algorithm.

Or

2. Find the convolution of two finite duration sequences

$$x(n) = \begin{cases} 1, & -1 \leq n \leq +1 \\ 0, & \text{otherwise} \end{cases} \quad \text{and} \quad h(n) = \begin{cases} 1, & -1 \leq n \leq 1 \\ 0, & \text{otherwise} \end{cases} \quad \text{using}$$

graphical method.

3. Realize the following IIR system function using cascade and parallel structures

$$H(z) = \frac{1}{(1 + rz^{-1})^3}$$

Or

4. Obtain an expression for the variance of the round-off quantization noise.
5. Explain Type—I frequency sampling method of designing FIR filter.

Or

6. Design a digital Chebyshev filter to meet the constraint.

$$0.8 \leq |H(e^{j\omega})| \leq 1, \quad 0 \leq \omega \leq 0.2\pi$$

$$|H(e^{j\omega})| \leq 0.2, \quad 0.6\pi \leq \omega \leq \pi$$

7. Explain the 3rd design iteration in FFT Processor with example.

Or

8. Draw the Block diagram of multi-bus architecture TMS Processor and explain the operation.

(4 × 10 = 40 marks)