(Pages: 2)

Namel SA EDUCATION OF THE REGISTRESS OF THE REGI

THIRD SEMESTER B.TECH. (ENGINEERING) [09 SCHEME] DEGREE EXAMINATION, NOVEMBER 2014

IT/CS 09 306/PTCS 09 305—SWITCHING THEORY AND LOGIC DESIGN

Time: Three Hours

Maximum: 70 Marks

Part A

Answer all questions.
Each question carries 2 marks.

- 1. Convert the Gray number 1110 to BCD.
- 2. Construct table for 3-input NOR gate.
- 3. List the gates with universal property.
- 4. What is a fault?
- 5. Write the truth table of a T-flip flop.

 $(5 \times 2 = 10 \text{ marks})$

Part B

Answer any four questions. Each question carries 5 marks.

6. Apply DeMorgan's theorems to the following:-

$$\overline{\overline{AB}}$$
 (CD + $\overline{\overline{EF}}$) ($\overline{\overline{AB}}$ + $\overline{\overline{CD}}$ and (A + $\overline{\overline{B}}$) ($\overline{\overline{C}}$ + D).

7. Using AND and OR gates implement the following expressions:

$$X = A (CD + B)$$
 and $X = ACD + B$.

- 8. Write notes on Test generation.
- 9. Explain parity generators.
- 10. Compare J-K flip flop and S-R flip-flop.
- 11. Explain the operation of parallel adders.

 $(4 \times 5 = 20 \text{ marks})$

Part C

Answer all questions.
Each question carries 10 marks.

12. (a) Use a Karnaugh map to reduce each expression to a minimum sum-of-products form :

$$X = A + B\overline{C} + CD$$
 and $X = \overline{AB} + A\overline{B} + \overline{CD} + C\overline{D}$.

- (b) Explain the rules and laws of Boolean algebra.
- 13. (a) Describe the universal property of NOR gate with suitable diagrams.

Or

- (b) Explain BCD-to-binary and binary-to-Gray code conversion with examples.
- 14. (a) Describe the procedure for finding the faults using Boolean difference method.

Or

- (b) Write notes on Fault-tolerance technique and Design for testability.
- 15. (a) Explain the operation of up-down counters.

Or

(b) Describe any two applications of shift registers.

 $(4 \times 10 = 40 \text{ marks})$