

C 61437

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Name.....

Reg. No.....



**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE  
EXAMINATION, APRIL 2014**

(2009 Scheme)

EC/PTEC 09 601—VLSI DESIGN

(Regular/Supplementary/Improvement)

Time : Three Hours

Maximum : 70 Marks

**Part A**

*Answer all questions.  
Each question carries 2 marks.*

1. What is Channel length modulation ?
2. Distinguish between depletion mode and enhancement mode MOSFET.
3. What is fault model ? Give an example.
4. What is a contrast curve ? Give its significance in VLSI fabrication.
5. What is a stick diagram ?

(5 × 2 = 10 marks)

**Part B**

*Answer any four questions.  
Each question carries 5 marks.*

6. Explain Pseudo NMOS logic.
7. Compare Static and Dynamic CMOS logic styles.
8. With neat sketch, explain the operation of a SRAM.
9. Explain Oxidation.
10. Explain twin tub process.
11. Draw the Layout of a two input CMOS NAND gate.

(4 × 5 = 20 marks)

**Part C**

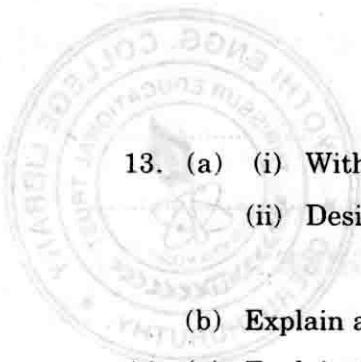
*Answer all questions.*

12. (a) Explain :
  - (i) Drain induced barrier lowering.
  - (ii) Velocity saturation.

Or

- (b) Explain the operation of a CMOS inverter and derive an expression for its propagation delay.

Turn over



- 13. (a) (i) With schematic explain the operation of a Carry bypass adder.
- (ii) Design a pass transistor based  $4 \times 1$  multiplexer.

Or

- (b) Explain any one test generation method with a suitable example.
14. (a) Explain diffusion, Oxidation and Ion Implantation.

Or

- (b) (i) Explain Optical lithography.
- (ii) Explain MOCVD technique.

15. (a) Explain LOCOS, SILO and SWAMI process.

Or

- (b) Explain  $\lambda$  based design rules.

(4 × 10 = 40 marks)