62950

Name : .....

Reg. No: .....

SEVENTH SEMESTER B.TECH (09 Scheme) DEGREE EXAMINATION-APRIL 2014

EC/PTEC 09 703 - ANALOG AND MIXED MOS CIRCUITS

Time: Three Hours **Maximum: 70 Marks**

PART — A

1. State any two limitations of CMOS technology.
2. What is a current source?
3. Why the trans conductance of the MOS device is not as large as BJT?
4. Mention any two advantages of Switched Capacitor Implementations.
5. What is the function of a loop filter in PLL?

(5 x 2 = 10 Marks)

PART - B

6. Explain the operation of a MOS switch.
7. Derive the expression for R_o and V_{min} of a cascode current mirror.
8. Draw the schematic of a active load current mirror.
9. With circuit schematic, explain the operation of switched capacitor integrator.
10. Explain the non ideal effects of PLL.
11. Explain the design of a CMOS comparator.

(4 x 5 = 20 Marks)

PART — C

12. (a) Explain the differential amplifier in detail.

(or)

(b) Discuss in detail about Band Gap Reference.

13. (a) Explain any one high gain amplifier architecture.

(or)

(b) Derive the frequency response of a differential amplifier .

14. (a) Draw the Schematic and explain operation of a Folded Cascode amplifier. Also derive its frequency response.

(or)

(b) Explain the design of CMOS two stage amplifier.

15. (a) Derive an expression for the output signal of a PLL. A PLL has a K_0 of 2π (1 kHz/V) , a k_v of $500s^{-1}$, and a free-running frequency of 500 Hz. For a constant input signal frequency of 250 Hz and 1 kHz, find V_o.

(or)

(b) Design a four quadrant analog multiplier using Gilbert Cell.

(10 x 4 = 40 Marks)

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